

# **EXHIBIT E**



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Balakrishnan et al.

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(54) **OFF-LINE CONVERTER WITH  
INTEGRATED SOFTSTART AND  
FREQUENCY JITTER**

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(51) Int. Cl.<sup>7</sup> ..... **H03K 3/017**

(52) U.S. Cl. .... **327/172; 327/143; 327/531;  
327/544**

(58) Field of Search ..... **327/142, 143,  
327/172, 173, 174, 175, 176, 530, 531,  
544**

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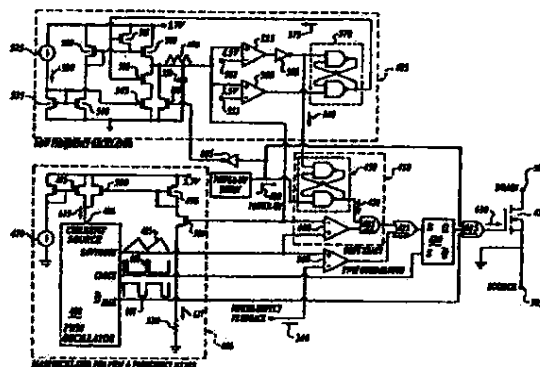
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(57) **ABSTRACT**

A pulse width modulated switch comprises a first terminal,  
a second terminal, and a switch that allows a signal to be  
transmitted between the first terminal and the second termi-  
nal according to a drive signal provided at a control input.  
The pulse width modulated switch also comprises a fre-  
quency variation circuit that provides a frequency variation  
signal and an oscillator that provides an oscillation signal  
having a frequency of that varies within a frequency range  
according to the frequency variation signal. The oscillator  
further provides a maximum duty cycle signal comprising a  
first state and a second state. The pulse width modulated  
switch further comprises a drive circuit that provides the  
drive signal when the maximum duty cycle signal is in the  
first state and a magnitude of the oscillation signal is below  
a variable threshold level.

18 Claims, 9 Drawing Sheets



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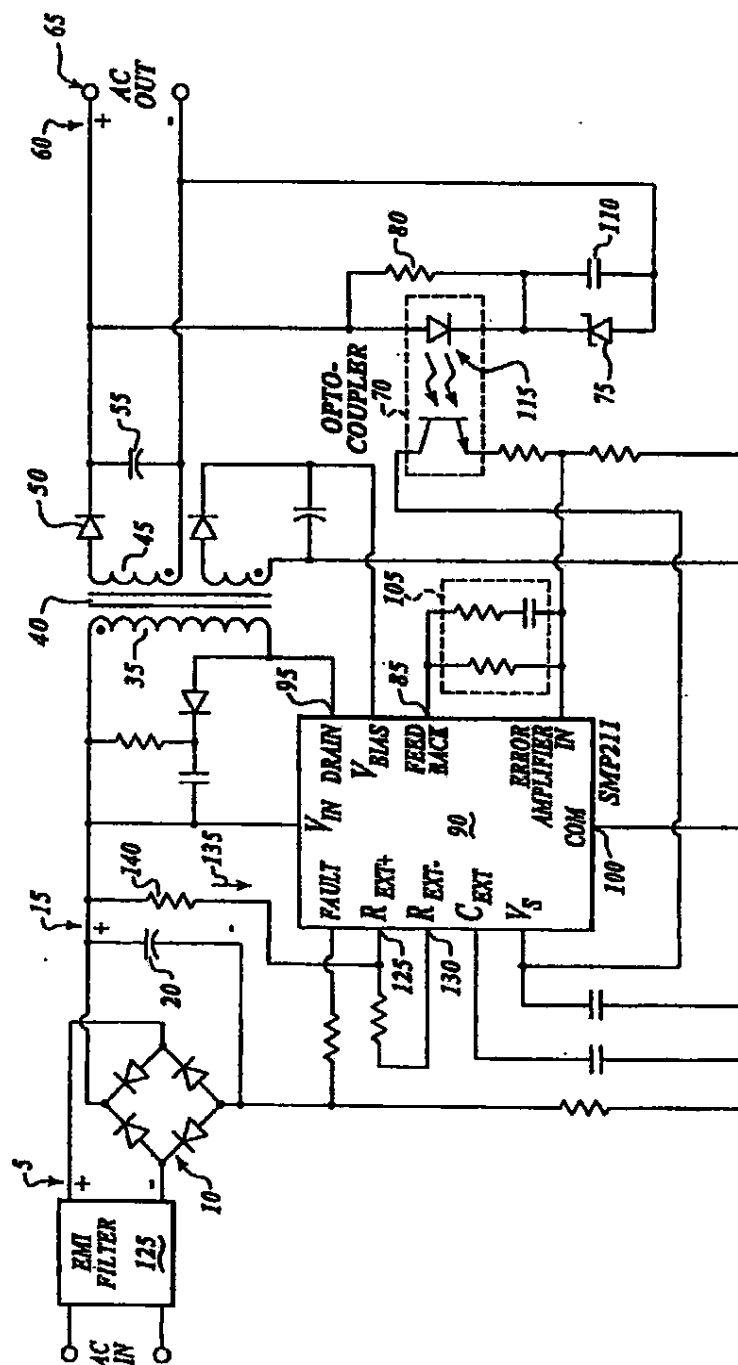


Fig. 1 (PRIOR ART)

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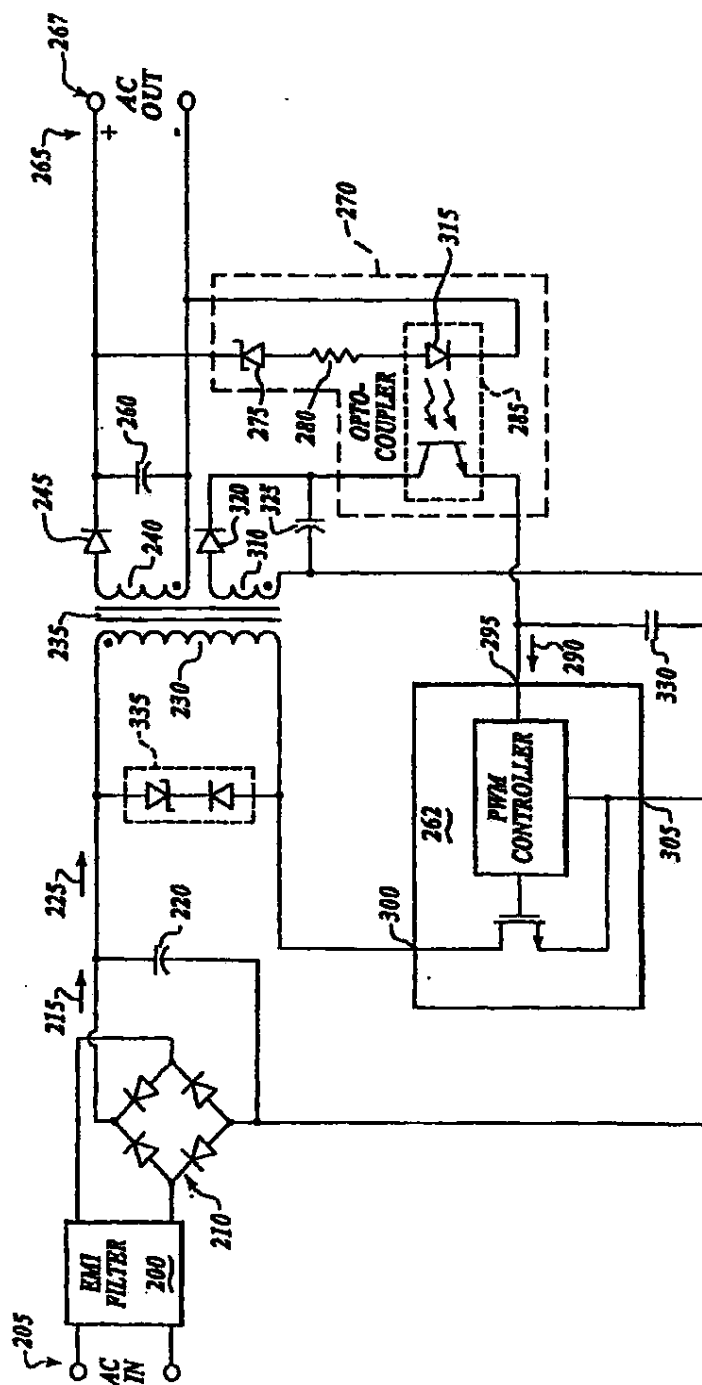


Fig. 2

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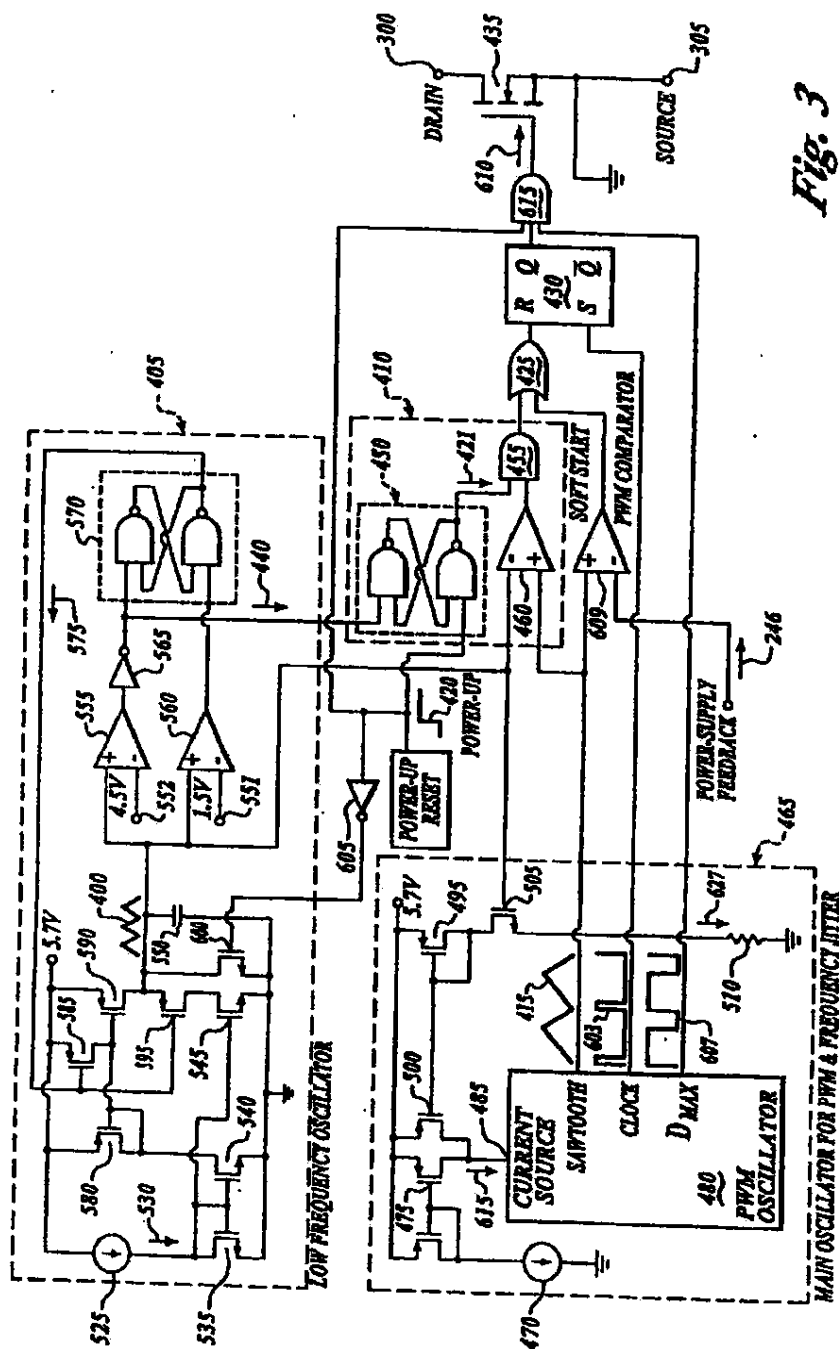


Fig. 3

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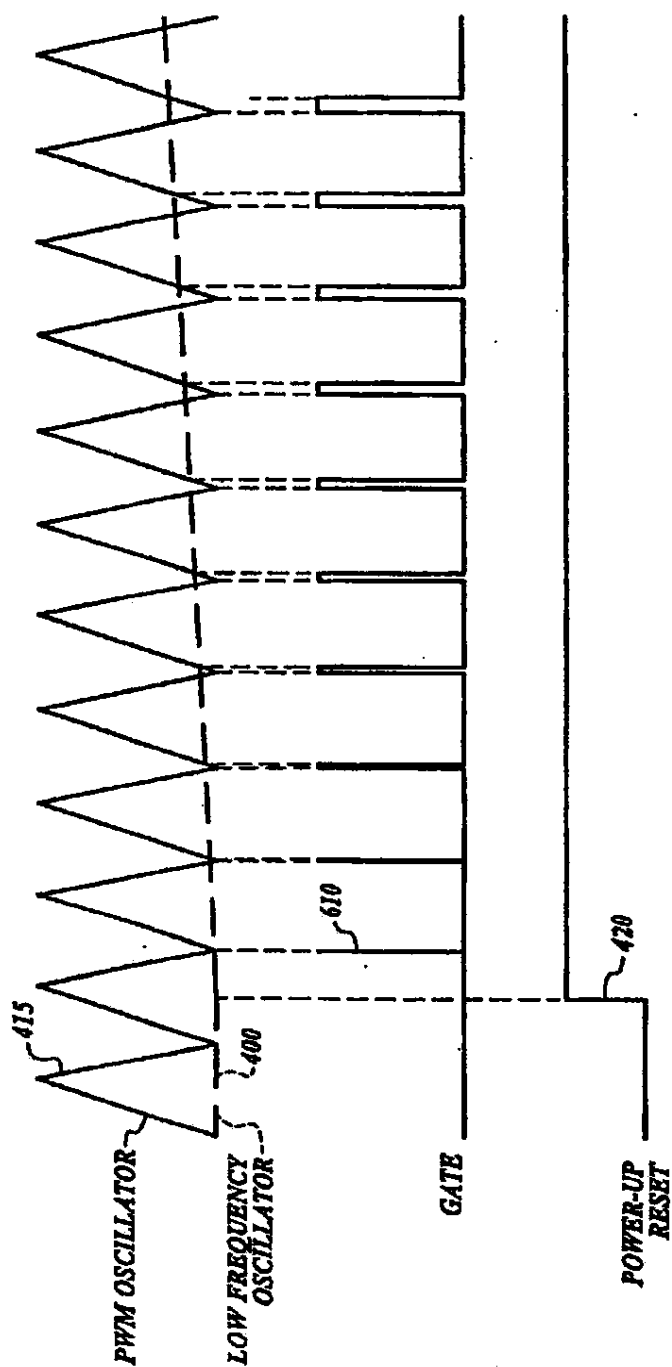


Fig. 4

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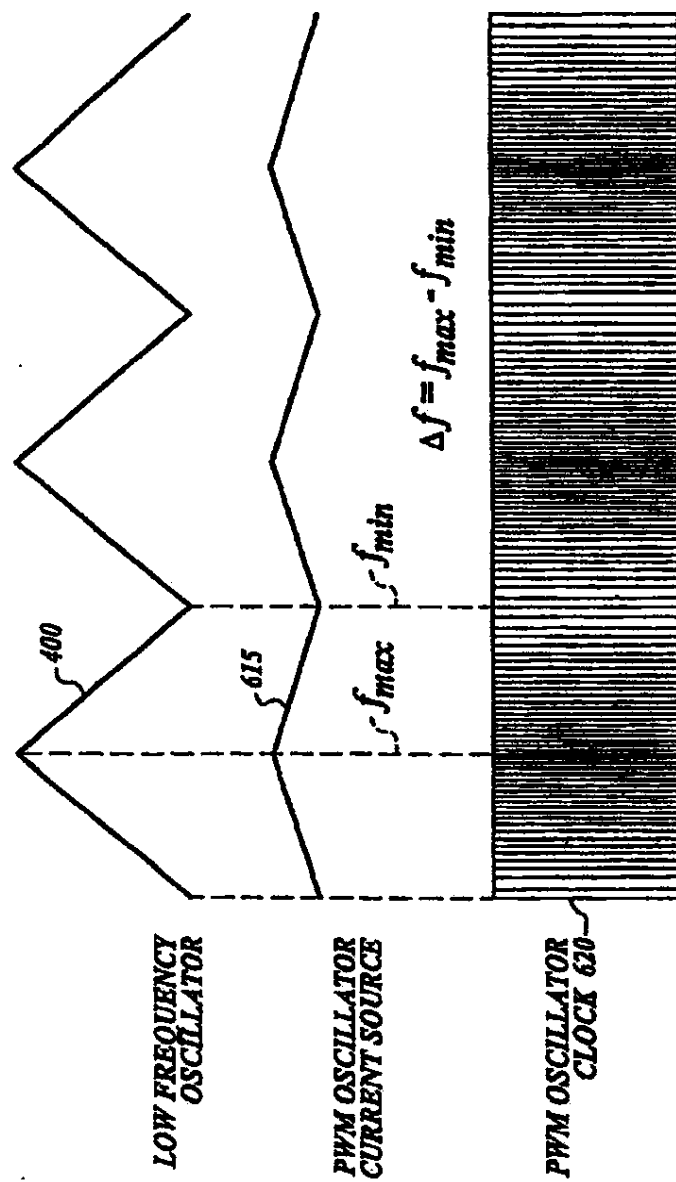
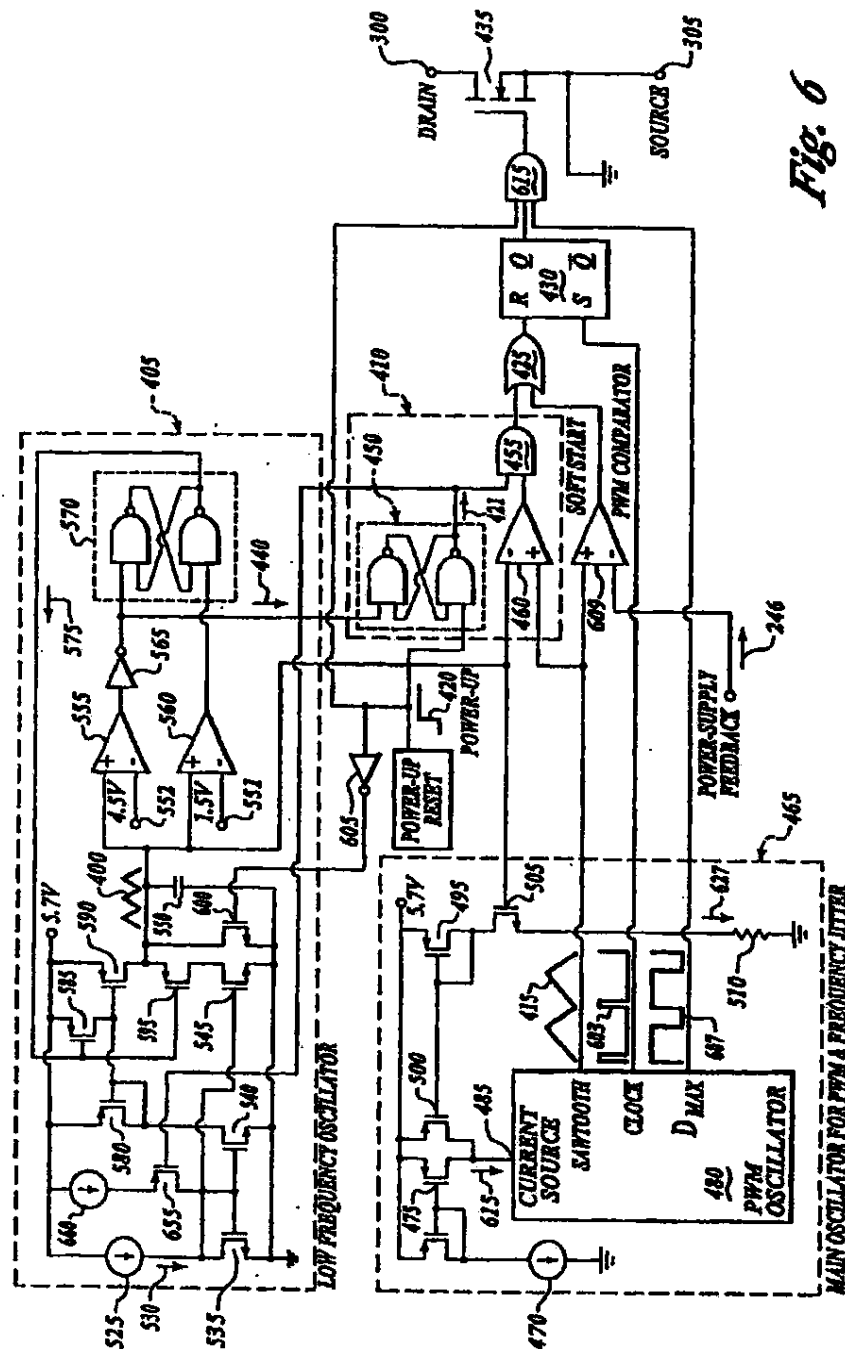


Fig. 5

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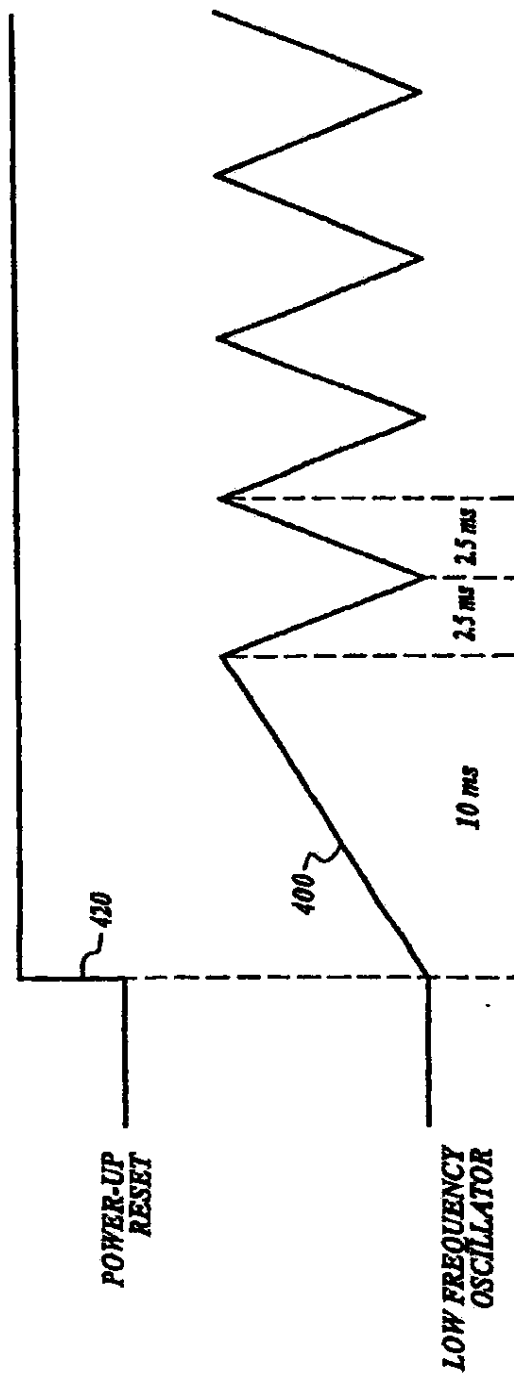
**Fig. 6**

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*Fig. 7*

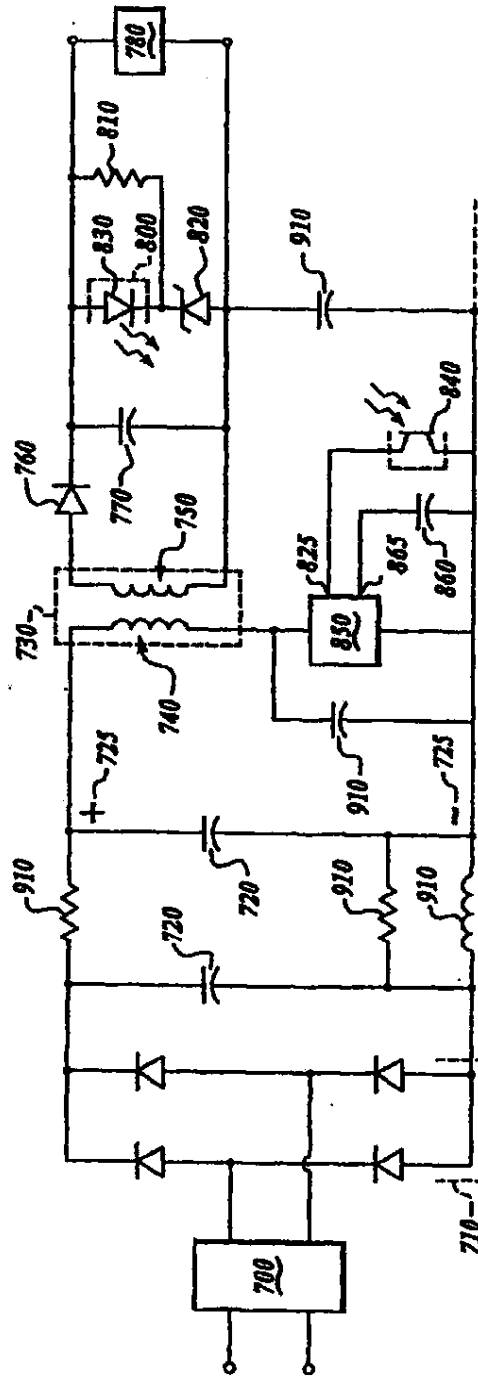
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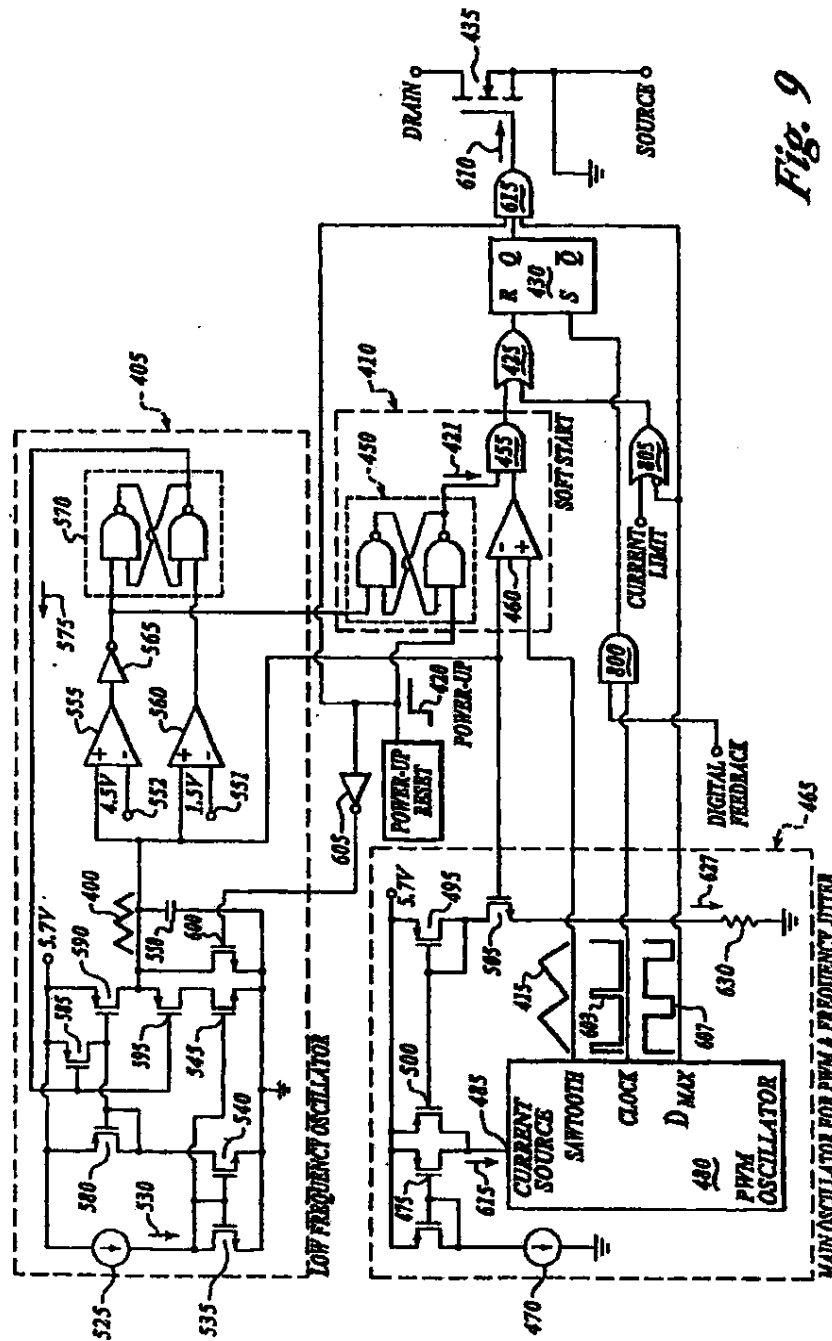


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**Fig. 9**

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# OFF-LINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER

## CROSS-REFERENCE TO RELATED APPLICATION

This is a Divisional of U.S. application Ser. No. 09/080,774, filed May 18, 1998, now U.S. Pat. No. 6,107,851.

## BACKGROUND

### 1. Field of the Invention

The field of the present invention pertains to the field of power supplies and among other things to the regulation of power supplies.

### 2. Background of the Invention

Power supplies that convert an AC mains voltage to a DC voltage for use by integrated electronic devices, amongst other devices, are known. The power supplies are required to maintain the output voltage, current or power within a regulated range for efficient and safe operation of the electronic device. Switches that operate according a pulse width modulated control to maintain the output voltage, current, or power of the power supply within a regulated range are also known. These switches utilize an oscillator and related circuitry to vary the switching frequency of operation of the switch, and therefore regulated the power, current or voltage that is supplied by the power supply.

A problem with utilizing pulse width modulated switches is that they operate at a relatively high frequency compared to the frequency of the AC mains voltage, which results in a high frequency signal being generated by the power supply. This high frequency signal is injected back into the AC mains input and becomes a component of the AC mains signal. The high frequency signals are also radiated by the power supply as electromagnetic waves. These high frequency signals add to the Electromagnetic Interference (EMI) of the power supply, and in fact are the largest contributors to the EMI of the power supply. The EMI generated by the power supply can cause problems for communications devices in the vicinity of the power supply and the high frequency signal which becomes a component of the AC mains signal will be provided to other devices in the power grid which also causes noise problems for those devices. Further, the radiated EMI by the power supply can interfere with radio and television transmissions that are transmitted over the air by various entities.

To combat the problem of EMI, several specifications have been developed by the Federal Communications Commission (FCC) in the United States and the European Community (EC) have established specification that specify the maximum amount of EMI that can be produced by classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing a power supply is minimizing the EMI provided by the power supply to levels with the acceptable limits of the various standards. Since, a power supply can be utilized in many different countries of the world, the EMI produced should be within the most stringent limits worldwide to allow for maximum utilization of the power supply.

A known way of minimizing the EMI provided by the power supply is by adding an EMI filter to the input of the power supply. An EMI filter generally utilizes at least one inductor, capacitor and resistor in combination. However, the greater EMI produced by the power supply the larger the

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components that are utilized as part of the EMI filter. The cost of the EMI filter is in large part determined by the size of the inductor and capacitor utilized. The longer the components, the higher the cost of the power supply. Further, simply utilizing an EMI filter does not address the radiated EMI.

Another problem associated with pulse width modulated switches results from operation of the power supply at start up. At start up, the voltage, current and power at the output of the power supply will essentially be zero. The pulse width modulated switch will then conduct for the maximum possible amount of time in each cycle of operation. The result of this is a maximum inrush current into the power supply. The maximum inrush current is greater than the current that is utilized during normal operation of the power supply. The maximum inrush current stresses the components of power supply and switch. Stress is specifically a problem for the switch, or transistor, the transformer of the power supply, and the secondary side components of the power supply. The stress caused by the maximum inrush current decreases the overall life of the power supply and increases the cost of the power supply because the maximum rating of the components used in the power supply is not destruct from the inrush currents will be greater than the maximum rating required for normal operation.

Further, when the pulse width modulated switch conducts for the maximum possible amount of time in each cycle of operation the voltage, current and power at the output of the power supply rise rapidly. Since the feedback circuit of the power supply often does not respond as fast as the operating frequency of the switch, the rapid rise of the voltage, current and power will often result in an overshoot of the maximum voltage in the regulation range which will cause damage to the device being supplied power by the power supply.

Referring to FIG. 1 a known power supply that attempts to minimize EMI and reduce startup stress is depicted. A rectifier 10 rectifies the filtered AC mains voltage 5, from EMI filter 120, input by the AC mains to generate a rectified voltage 15. Power supply capacitor 20 then generates a substantially DC voltage with a ripple component. The rectified voltage 15 with ripple component is provided to the primary winding 35 of transformer 40 that is used to provide power to secondary winding 45. The output of secondary winding 45 is provided to secondary rectifier 50 and secondary capacitor 55 that provide a secondary DC voltage 60 at the power supply output 65 to the device that is coupled to the power supply.

In order to maintain the secondary DC voltage within a regulate range a feedback loop including an optocoupler 70, zener diode 75 and a feedback resistor 80 provides a signal indicative of the voltage at the power supply output 65 to feedback pin 85 of pulse width modulated switch 90. The voltage magnitude at the feedback terminal is utilized to vary the duty cycle of a switch coupled between the drain terminal 95 and common terminal 100 of the pulse width modulated switch 90. By varying the duty cycle of the switch the average current flowing through the primary winding and therefore the energy stored by the transformer 40 which in turn controls the power supplied to the power supply output 65 is kept within the regulated range. A compensation circuit 105 is coupled to the feedback pin 85 in order to lower the bandwidth of the frequency of operation of the pulse width modulator.

Inrush currents are minimized at start up by use of soft start capacitor 110. Soft start functionality is termed to be a functionality that reduces the inrush currents at start up. At

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this instant a current begins to flow through feedback resistor 80 and thereby into soft start capacitor 110. As the voltage of soft start capacitor 110 increases slowly, current will flow through light emitting diode 115 of optocoupler 70 thereby controlling the duty cycle of the switch. Once the voltage of the soft start capacitor 110 reaches the reverse breakdown voltage of zener diode 75 current will flow through zener diode 75. The approach described above will reduce the inrush currents into the power supply, however, it will be several cycles before the light emitting diode 115 will begin conducting. During the several cycles the maximum inrush current will still flow through the primary winding and other secondary side components. During these cycles the transformer may saturate, and therefore the transformer may have to be designed utilizing a higher core size than would be required for normal operation even with the use of soft start capacitor as in FIG. 1.

To reduce the EMI output by the power supply an EMI filter 120 is utilized. Additionally, pulse width modulated switch 90 is equipped with frequency oscillation terminals 125 and 130. Frequency oscillation terminal 125 and 130 receive a jitter current 135 that varies according to the ripple component of substantially DC voltage 25. The jitter current 135 is used to vary the frequency of the saw-toothed waveform generated by the oscillator contained in the pulse width modulated switch 90. The saw toothed waveform generated by the oscillator is compared to the feedback provided at the feedback pin 85. As the frequency of the saw toothed waveform varies, so will the switching frequency of the switch coupled between the drain and common terminal. This allows the switching frequency of the switch to be spread over a larger bandwidth, which minimizes the peak value of the EMI generated by the power supply at each frequency. By reducing the EMI the ability to comply with government standards is increased, because the government standards specify quasi-peak and average values at given frequency levels. Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter.

A problem associated with the EMI reduction scheme described with respect to FIG. 1 is that the ripple component will have variances due to variations in the line voltage and output load. Additionally, since the ripple may vary, design and the component value of EMI resistor 140 is difficult to determine and correspondingly design of the power supply becomes problematic.

#### SUMMARY OF THE INVENTION

In one embodiment the present invention comprises a pulse width modulated switch comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated circuit further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

Another embodiment of the present invention comprises a pulse width modulated switch comprising a switch comprising a control input, the switch allowing a signal to be

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transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state, a drive circuit that provides the drive signal, and a soft start circuit that provides a signal instructing said drive circuit to disable the drive signal during at least a portion of said on-state of the maximum duty cycle.

In an alternate embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a drive circuit that provides the drive signal and a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal.

In yet another embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a frequency variation circuit that provides a frequency variation signal, and a drive circuit that provides a drive signal for a maximum time period of a time duration cycle. The time duration of the cycle varies according to the frequency variation signal.

In the above referenced embodiments the pulse width modulated switch or regulation circuit may comprise a monolithic device.

An object of an aspect of the present invention is directed to a pulse width modulated switch that has integrated soft start capabilities.

Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities.

Yet another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities and integrated soft start capabilities.

A further object of an aspect of the present invention is directed toward a low cost regulated power supply that has both soft start and frequency variation capabilities.

This and other objects and aspects of the present invention are taught, depicted and described in the drawings and the description of the invention contained herein.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a known power supply utilizing a pulse width modulated switch, and external soft start, and frequency jitter functionality.

FIG. 2 is a presently preferred power supply utilizing an pulse width modulated switch according to the present invention.

FIG. 3 is a presently preferred pulse width modulated switch according to the present invention.

FIG. 4 is a timing diagram of the soft start operation of the presently preferred pulse width modulated switch according to the present invention.

FIG. 5 is a timing diagram of the frequency jitter operation of the presently preferred pulse width modulated switch according to the present invention.

FIG. 6 is an alternate presently preferred pulse width modulated switch according to the present invention.

FIG. 7 is a timing diagram of the operation of the alternate presently preferred pulse width modulated switch of FIG. 6 according to the present invention.

FIG. 8 is a presently preferred power supply utilizing a regulation circuit according to the present invention.

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FIG. 9 is a presently preferred regulation circuit according to the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, EMI filter 200 is coupled to an AC mains voltage 205. The AC mains voltage 205 is rectified by rectifier 210. The rectified voltage 215 is provided to power supply capacitor 220 which provides a substantially DC voltage 225. The substantially DC voltage 225 is provided to the primary winding 230 of transformer 235 which stores the energy provided to the primary winding 230. When the primary winding 230 is no longer receiving energy, energy is delivered by the transformer 235 to the secondary winding 240. The voltage induced across the secondary winding 240 is rectified by rectifier 245 and then transformed into secondary substantially DC voltage 265 by secondary capacitor 260 and provided to the power supply output 267.

Energy is no longer provided to the primary winding 230 when the pulse width modulated switch 262, which is coupled to the primary winding 230, ceases conduction. Pulse width modulated switch 262 is a switch that is controlled by a pulse width modulated signal. Pulse width modulated switch 262 conducts and ceases conduction according to a duty cycle, that is in part determined by feedback from the power supply output 267. Pulse width modulated switch 262 is a switch that operates according to pulse width modulated control. Feedback to the pulse width modulated switch 262 is accomplished by utilization of feedback circuit 270, which is presently preferred to comprise a zener diode 275 in series with a resistor 280 and optocoupler 285. Optocoupler 285 provides a feedback current 290 to feedback terminal 295 of pulse width modulated switch 262. The feedback current is utilized to vary the duty cycle of a switch coupled between the first terminal 300 and second terminal 305 and thus regulate the output voltage, current or power of the power supply.

Although, it is presently preferred that the output voltage is utilized for feedback, the present invention is also capable of utilizing either the current or power at the power supply output 267 without departing from the spirit and scope of the present invention.

A portion of the current supplied at the feedback terminal 295 is utilized to supply bias power for operation of the pulse width modulated switch 262. The remainder of the current input at the feedback terminal 295 is utilized to control the duty cycle of the pulse width modulated switch 262, with the duty cycle being inversely proportional to the feedback current.

A bias winding 310 is utilized to bias optocoupler 285 so that a feedback current can flow when light emitting diode 315 of optocoupler 285 conducts. The power supplied by the bias winding 310 is also used to charge pulse width modulation capacitor 330, the energy from which is utilized to power the pulse width modulated switch 262.

Overvoltage protection circuit 335 is utilized to prevent overvoltages from propagating through to the transformer 235.

Pulse width modulated switch 262 is supplied power during start up of the power supply by current flowing into the first terminal 300. An embodiment of one type of apparatus and method for designing a configuration for providing power to pulse width modulated switch through first terminal 300 is disclosed in commonly owned U.S. Pat. No. 5,014,178 which is incorporated herein by reference in its entirety.

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The drain terminal 300, source terminal 305 and feedback terminal 295 are the electrical input and/or output points of the pulse width modulated switch 262. They need not be part of a monolithic device or integrated circuit, unless the pulse width modulated switch 262 is implemented utilizing a monolithic device or integrated circuit.

Pulse width modulated switch 262 also may have soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of pulse width modulated switch 262. The power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, pulse width modulated switch 262 operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, pulse width modulated switch 262 may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch 262 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. 1 in that the frequency range of the presently preferred pulse width modulated switch 262 is known and fixed, and is not subject to the line voltage or load magnitude variations. At low powers, those less than approximately ten (10) watts, the common mode choke which is often utilized as part of the EMI filter 200 can be replaced with inductors or resistors.

As can be seen when comparing the power supply of FIG. 1 to that of FIG. 2 the number of components utilized is reduced. This reduces the overall cost of the power supply as well as reducing its size.

Referring to FIG. 3, frequency variation signal 400 is utilized by the pulse width modulated switch 262 to vary its switching frequency within a frequency range. The frequency variation signal 400 is provided by frequency variation circuit 405, which preferably comprises an oscillator that operates at a lower frequency than main oscillator 465. The frequency variation signal 400, is presently preferred to be a triangular waveform that preferably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal 400 is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal.

The frequency variation signal 400 is provided to soft start circuit 410. During operation soft start circuit 410 is also provided with pulse width modulation frequency signal 415 and power up signal 420. Soft start enable signal 421 goes high at power up and remains high until oscillator signal 400 reaches its peak value for the first time. Soft start circuit 410 will provide a signal to or-gate 425 to reset latch 430 thereby deactivating conduction by the switch 435, which is presently preferred to be a MOSFET. Soft start circuit 410 will instruct switch 435 to cease conduction when the soft start enable signal 421 is provided and the magnitude of the frequency variation signal 400 is less than the magnitude of pulse width modulation signal 415. In other words, start up circuit 410 will allow the switch 435 to conduct as long as soft start enable signal is high and the magnitude of the pulse width modulation signal 415 is below the magnitude of frequency variation signal 400 as depicted in FIG. 4. In this way, the inrush current at startup will be limited for all cycles of operation, including the first

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cycle. By limiting the inrush current during all cycles of startup operation, the maximum current through each of the components of the power supply is reduced and the maximum current rating of each component can be decreased. The reduction in the ratings of the components reduces the cost of the power supply. Soft start signal 440 will no longer be provided by the frequency variation circuit 405 when the frequency variation signal 400 reaches its peak magnitude.

Operation of soft start circuit 410 will now be explained. Soft start circuit 410 comprises a soft start latch 450 that at its set input receives the power up signal 420 and its reset input receives the soft start signal 440. Soft start enable signal 421 is provided to one input of soft start and-gate 455 while the other input of soft start and-gate 455 is provided with an output from soft start comparator 460. The output of soft start comparator 460 will be high when the magnitude of frequency variation signal 400 is less than the magnitude of pulse width modulation oscillation signal 415.

The pulse width modulated switch 262 depicted in FIG. 3 also has frequency jitter functionality to help reduce the EMI generated by the power supply and pulse width modulated switch 262. Operation of the frequency jitter functionality will now be explained. Main oscillator 465 has a current source 470 that is mirrored by mirror current source 475. Main oscillator drive current 615 is provided to the current source input 485 of PWM oscillator 480. The magnitude of the current input into current source input 485 of PWM oscillator 480 determines the frequency of the pulse width modulation oscillation signal 415 which is provided by PWM oscillator 480. In order to vary the frequency of pulse width modulation oscillation signal 415, an additional current source 495 is provided within main oscillator 465. The additional current source 495 is mirrored by additional current source mirror 500. The current provided by additional current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases so does the voltage at the source of main oscillator transistor 505, due to the increasing voltage at the gate of main oscillator transistor and the relatively constant voltage drop between the gate and source of the main oscillator transistor 505. As the voltage at the source of main oscillator transistor 505 increases so does the current flowing through the main oscillator resistor 510. The current flowing through main oscillator resistor 510 is the same as the current flowing through additional current source 495 which is mirrored by additional current source mirror 500. Since, the presently preferred frequency variation signal 400 is a triangular waveform having a fixed period, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency would linearly rise to a peak and then immediately fall to its lowest value. In this way, the current provided to current source input 485 of PWM oscillator 480 is varied in a known fixed range that allows for easy and accurate frequency spread of the high frequency current generated by the pulse width modulated switch. Further, the variance of the frequency is determined by the magnitude of the current provided by additional current source mirror 500, which is in turn a function of the resistance of main oscillator resistor 510.

Frequency variation circuit 405 includes a current source 525 that produces a fixed magnitude current 530 that determines the magnitude of the frequency of the frequency variation signal 400. Although, the presently preferred cur-

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rent 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current, if a variable current is generated the frequency spread would not be fixed in time but would vary with the magnitude of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirrored by second transistor 540 and fed into third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of frequency variation circuit capacitor 550. Frequency variation circuit capacitor 550 is presently preferred to have a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of the pulse width modulated switch 262. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 560. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage 552 which is presently preferred to be four point five (4.5) volts. The output of lower limit comparator 560 will be high when the magnitude of frequency variation signal 400 exceeds lower threshold voltage 557 which is presently preferred to be one point five volts (1.5) volts. The output of upper limit comparator 555 is provided to the frequency variation circuit inverter 565 the output of which is provided to the reset input of frequency variation circuit latch 570. The set input of frequency variation circuit latch 570 receives the output of lower limit comparator 560. In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between upper threshold 552, 4.5 volts, and the lower threshold 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation signal 400 exceeds upper level threshold 552. This means that the reset input will receive a high signal until the magnitude of the frequency variation signal 400 rises above the upper threshold signal 552.

The charge signal 575 output by frequency variation circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal 552. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 585 and 595 current can flow into frequency variation circuit capacitor 550, which steadily charges frequency variation circuit capacitor 550 and increases the magnitude of frequency variation signal 400. The current that flows into frequency variation circuit capacitor 550 is derived from current source 525 because the current through transistor 590 is mirrored from transistor 580, which is mirrored from transistor 535.

During power up, when power-up signal 420 is low, the output of inverter 605 is high which turns on transistor 600 causing frequency variation signal 400 to go low. The frequency variation signal 400 is presently preferred to start from its lowest level to perform the soft start function during its first cycle of operation.

Steady-state operation of the pulse width modulated switch 262, i.e. non start up operation, will now be described. PWM oscillator 480 provides pulse width modulation oscillation signal 415 to pulse width modulation comparator 609, the output of which will be high when the magnitude of pulse width modulation signal 415 is greater than the magnitude of a feedback signal 296 which is a function of the input provided at feedback terminal 295. When the output of pulse width modulation comparator 609 is high or-gate 425 is triggered to go high, which in turn resets pulse width modulation latch 430, removing the on signal from the control input switch 435, thereby turning off

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switch 435. Pulse width modulation latch 430 is set by clock signal 603, which is provided at the beginning of each cycle of pulse width modulation oscillator 480. Drive circuit 615, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch 430, power up signal 428, and maximum duty cycle signal 607. As long as each one of the signals is high, drive signal 610 is provided to the gate of MOSFET 435, which is coupled between first terminal 300 and second terminal 305 of the pulse width modulated switch 262. When any of the output of pulse width modulation latch 430, power up signal 428, or maximum duty cycle signal 607 goes low drive signal 610 is no longer provided and switch 435 ceases conduction.

Referring to FIG. 4, frequency variation signal 400 preferably has a period, which is greater than that of pulse width modulated oscillation signal 415. The presently preferred period for frequency variation signal 400 is twenty (20) milliseconds, in order to allow for a smooth start up period which is sufficiently longer than the period of pulse width modulated signal 415 which is presently preferred to be ten (10) microseconds. Drive signal 610 will be provided only when the magnitude of pulse width modulated signal 415 is less than the magnitude of frequency variation signal 400. Further, frequency variation signal 400 will be preferably initiated starting from low voltage when power up signal 420 is provided.

Referring to FIG. 5, frequency variation signal 400 which is presently preferred to have a constant period is provided to the main oscillator 465. The magnitude of the pulse width modulator current 615 will be approximately be the magnitude of frequency variation signal 400 divided by the resistance of resistor 510 plus the magnitude of the current produced by current source 470. In this way the pulse width modulator current 615 will vary with the magnitude of the frequency variation signal 400. The result is that the frequency of pulse width modulation signal is varied according to the magnitude of this current. It is presently preferred that the pulse width modulator current source produces a constant current having a magnitude of twelve point one (12.1) microamperes, and that frequency variation signal induced current 627 varies between zero (0) and eight hundred (800) nanoperes. Thereby spreading the frequency of operation of the pulse width modulation oscillator 480 and reducing the average magnitude and the quasi-peak magnitude at all frequency levels of the EMI generated by the power supply.

Referring to FIG. 6, an alternate presently preferred pulse width modulated switch 262 includes all of the same components as described with respect to FIG. 3. In addition to these components, a second frequency variation circuit current source 660 and transistor 655 are added to the frequency variation circuit 405. Transistor 655 is activated only when the output of soft start latch 450 goes low. When transistor 655 is activated the current provided to the frequency variation circuit 405 increases as does the frequency of frequency variation signal 400. However, transistor 655 will only be turned on when the output of soft start latch 450 goes low, i.e. when the magnitude of frequency variation signal 400 first reaches the upper threshold after power up. The period of frequency variation signal 400 will then increase after its first half cycle. This will decrease the period of the cycle during which the frequency is spread, without decreasing the frequency range. The benefit of the decreased cycle period will further decrease the quasi-peak levels of the EMI due to spending less time at each frequency level.

Referring to FIG. 7, operation of the frequency variation circuit 405 of FIG. 6 is depicted. Frequency variation signal

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405 will preferably have a period of ten (10) milliseconds for its first half cycle. After that, when the transistor 655 is turned on the period is preferably decreased to five (5) milliseconds. Pulse width modulated switch 262 is presently preferred to be a monolithic device.

Referring to FIG. 8, a power supply comprises a bridge rectifier 710 that rectifies an input AC mains voltage. Power supply capacitors 720 charge with the rectified AC mains voltage to maintain an input DC voltage 725. A presently preferred range for input DC voltage 725 is approximately one hundred (100) to four hundred (400) volts to allow for operation based upon worldwide AC mains voltages which range between eighty five (85) and two hundred sixty five (265) volts. The presently preferred power supply also includes harmonic filter components 910 which in combination with capacitors 720 reduce the harmonic current injected back into the power grid. Transformer 730 includes a primary winding 740 magnetically coupled to secondary winding 750. The secondary winding 750 is coupled to a diode 760 that is designed to prevent current flow in the secondary winding 750 when the regulation circuit 850 is conducting (on-state). A capacitor 770 is coupled to the diode 760 in order to maintain a continuous voltage on a load 780 which has a feedback circuit coupled to it. A presently preferred feedback circuit comprises an optocoupler 800 and zener diode 820. The output of optocoupler 800 is coupled to the feedback terminal 825 of regulation circuit 850. The presently preferred regulation circuit 850 switches on and off at a duty cycle that is constant at a given input DC voltage 740. A regulation circuit power supply bypass capacitor 860 is coupled to and supplies power to regulation circuit 850 when the regulation circuit 850 is in the on-state.

Operation of the power supply will now be described. An AC mains voltage is input through EMI filter 700 into bridge rectifier 710 which provides a rectified signal to power supply capacitors 720 that provide input DC voltage 725 to primary winding 740. Regulation circuit 850, which preferably operates at a constant frequency and about constant duty cycle at a given input DC voltage 725, allows current to flow through primary winding 740 during its on state of each switching cycle and acts as open circuit in its off state. When current flows through primary winding 740 transformer 730 is storing energy, when no current is flowing through primary winding 740 any energy stored in transformer 730 is delivered to secondary winding 750. Secondary winding 750 then provides the energy to capacitor 770. Capacitor 770 delivers power to the load 780. The voltage across the load 780 will vary depending on the amount of energy stored in the transformer 730 in each switching cycle which is in turn dependent on the length of time current is flowing through primary winding 740 in each switching cycle which is presently preferred to be constant at a given input DC voltage 725. The presently preferred regulation circuit 850 allows the voltage delivered to the load to be maintained at a constant level.

It is presently preferred that the sum of the voltage drop across optocoupler 800 and the reverse break down voltage of zener diode 820 is approximately equal to the desired threshold level. When the voltage across the load 780 reaches the threshold level, current begins to flow through the optocoupler 800 and zener diode 820 that in turn is used to disable the regulation circuit 850. Whenever regulation circuit 850 is in the off-state the regulation circuit power supply bypass capacitor 860 is charged to the operating supply voltage, which is presently preferred to be five point seven (5.7) volts by allowing a small current to flow from bypass terminal 865 to the regulation circuit power supply

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bypass capacitor 860. Regulation circuit power supply bypass capacitor 860 is used to supply power to operate regulation circuit 850 when it is in the on-state.

When the regulation circuit 850 is disabled, an open circuit condition is created in primary winding 740 and transformer 730 does not store energy. The energy stored in the transformer 730 from the last cycle of regulation circuit 850 is then delivered to secondary winding 750 which in turn supplies power to the load 780. Once the remaining energy in transformer 750 is delivered to the load 780 the voltage of the load 780 will decrease. When the voltage at the load 780 decreases below the threshold level, current ceases to flow through optocoupler 800 and regulation circuit 850 resumes operation either instantaneously or nearly instantaneously.

The presently preferred regulation circuit 850 has a current limit feature. The current limit turns off the regulation circuit 850, when the current flowing through the regulation circuit 850 rises above a current threshold level. In this way regulation circuit 850 can react quickly to changes such as AC ripple that occur in the rectified AC mains voltage, and prevents the propagation of the voltage changes to the load. The current limit increases the responsiveness of the regulation circuit to input voltage changes and delivers constant power output independent for the AC mains input voltage.

Although the presently preferred power supply of FIG. 8 utilizes current mode regulation and a feedback circuit that includes an optocoupler and zener diode, the present invention is not to be construed as to be limited to such a feedback method or circuit. Either current or voltage mode regulation may be utilized by the present invention without departing from the spirit and scope of the present invention so long as a signal indicative of the power supplied to the load is supplied to the feedback terminal 825 of the regulation circuit 850. Additionally, although the presently preferred power supplies both utilize an optocoupler and zener diode as part of feedback circuits other feedback circuits may be utilized by the present invention without departing from the spirit and scope of the present invention.

Regulation circuit 850 also may have integrated soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of regulation circuit 850. A power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch 262 for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, regulation circuit 850 operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, regulation circuit 850 may also have frequency jitter functionality. That is, the switching frequency of the regulation circuit 850 varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. 1 in that the frequency range of the presently regulation circuit 850 is known and fixed, and is not subject to the line voltage or load magnitude variations.

Referring to FIG. 9, frequency variation circuit 405 and main oscillator 465 function as described with respect to FIG. 3. In operation it is the variance of the high and low states of maximum duty cycle signal 607 that generates the frequency jitter functionality of the regulation circuit 850. A presently preferred regulation circuit 850 and its steady-state operation is depicted and described in copending patent application Ser. No. 09/032,520 which is hereby incorporated by reference in its entirety.

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The regulation circuit of FIG. 9 can be modified to include a second current source to further increase the period of main oscillation signal 415 which achieves the same result and function as described with respect of FIGS. 6 and 7.

The soft start functionality of the presently preferred regulation circuit 850 of FIG. 9, will shorten the on-time of switch 435 to less than the time of the maximum duty cycle signal 607 as long as the soft start enable signal 421 is provided and the magnitude of frequency variation signal 400 is less than the magnitude of main oscillation signal 415.

The presently preferred regulation circuit 850 preferably comprises a monolithic device.

While the embodiments, applications and advantages of the present invention have been depicted and described, there are many more embodiments, applications and advantages possible without deviating from the spirit of the inventive concepts described herein. Thus, the inventions are not to be restricted to the preferred embodiments, specification or drawings. The protection to be afforded this patent should therefore only be restricted in accordance with the spirit and intended scope of the following claims.

What is claimed is:

1. A pulse width modulated switch comprising

a first terminal;

a second terminal;

a switch comprising a control input, the switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state;

a drive circuit that provides said drive signal according to said maximum duty cycle signal; and

a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle.

2. The pulse width modulated switch of claim 1 wherein said a first terminal, said second terminal, said switch, said oscillator, said drive circuit and said soft start circuit comprise a monolithic device.

3. The pulse width modulated switch of claim 1 further comprising an additional oscillator that provides a soft start signal to said soft start circuit, and wherein when said soft start signal is removed said soft start circuit ceasing operation.

4. The pulse width modulated circuit of claim 3 wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation oscillation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

5. The pulse width modulated switch of claim 1 further comprising a frequency variation circuit that provides a frequency variation signal, wherein said oscillator provides an oscillation signal and wherein said soft start circuit provides said signal instructing said drive circuit to disable said drive signal when a magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

6. The pulse width modulated switch of claim 5 wherein said oscillator comprises an input that receives said frequency signal and said oscillation signal comprises a frequency range, and wherein said frequency of said oscillation

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signal varies within said frequency range according to a magnitude of said frequency variation signal.

7. The pulse width modulated switch of claim 6 wherein said oscillator further comprises a current source, wherein said frequency of said oscillation signal is a function of a sum of a magnitude of a current provided by said current source and said magnitude of said frequency variation signal.

8. The pulse width modulated switch of claim 1 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said pulse width modulated switch; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

9. A regulation circuit comprising

a first terminal;

a second terminal;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

a drive circuit that provides said drive signal for a maximum time period of a cycle; and

a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period.

10. The regulation circuit of claim 9 further comprising an oscillator that provides a maximum duty cycle signal to said drive circuit, said maximum duty cycle signal comprising an on-state for said maximum time period.

11. The regulation circuit of claim 10 further comprising a frequency variation circuit that provides a frequency variation signal, wherein said oscillator provides an oscillation signal and wherein said soft start circuit provides said signal instructing said drive circuit to disable said drive

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signal when a magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

12. The regulation circuit of claim 9 further comprising an additional oscillator that provides a soft start signal to said soft start circuit, and wherein when said soft start signal is removed said soft start circuit ceases operation.

13. The regulation circuit of claim 12 wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said additional oscillation signal, and an inverter that receives said comparator signal and provides said soft start signal.

14. The regulation circuit of claim 9 further comprising a frequency variation circuit that provides a frequency variation signal and wherein said maximum time period varies according to a magnitude of said frequency variation signal.

15. The regulation circuit of claim 9 further comprising a feedback terminal and wherein when a signal is received at said feedback terminal said drive signal is discontinued for at least one cycle.

16. The regulation circuit of claim 9 wherein said first terminal, said second terminal, said oscillator and said soft start circuit comprise a monolithic device.

17. The regulation circuit of claim 16 further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level.

18. The regulation circuit of claim 9 further comprising

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving a substantially DC signal from said power supply capacitor, said second terminal of said first winding coupled to said first terminal of said regulation circuit; and

a second winding magnetically coupled to said first winding, said first winding capable of being coupled to a load.

\* \* \* \* \*

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# **EXHIBIT F**



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Balakrishnan et al.

(10) Patent No.: **US 6,249,876 B1**  
(45) Date of Patent: **Jun. 19, 2001**

(54) **FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY**

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patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

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(51) Int. Cl.<sup>7</sup> **G06F 1/04**

(52) U.S. Cl. **713/501; 713/300; 713/503**

(58) Field of Search **713/300, 320,**  
**713/322, 500, 501, 503**

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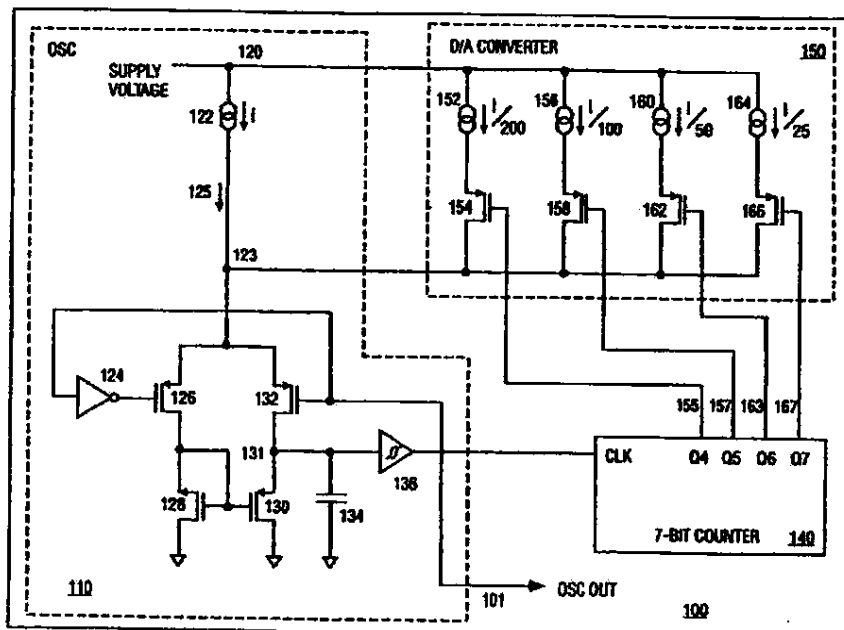
**Primary Examiner**—**Dennis M. Butler**

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(57) **ABSTRACT**

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is connected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

**32 Claims, 6 Drawing Sheets**



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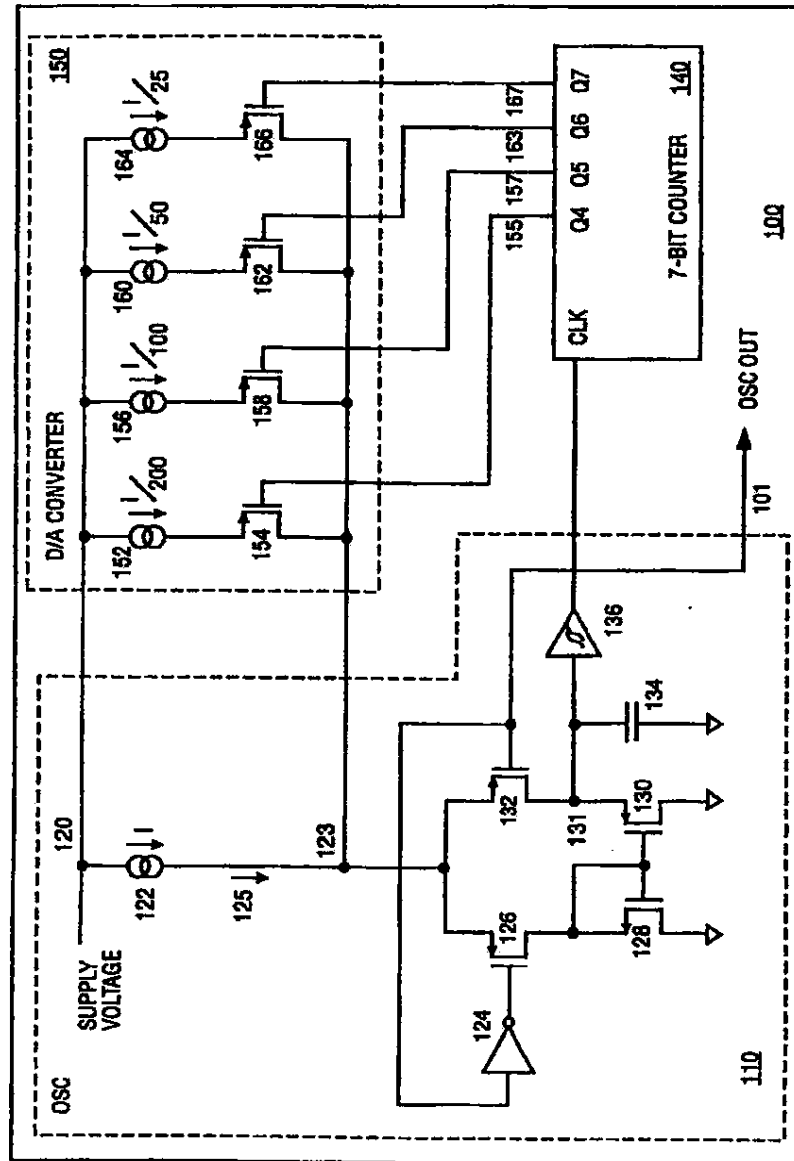


FIG. 1

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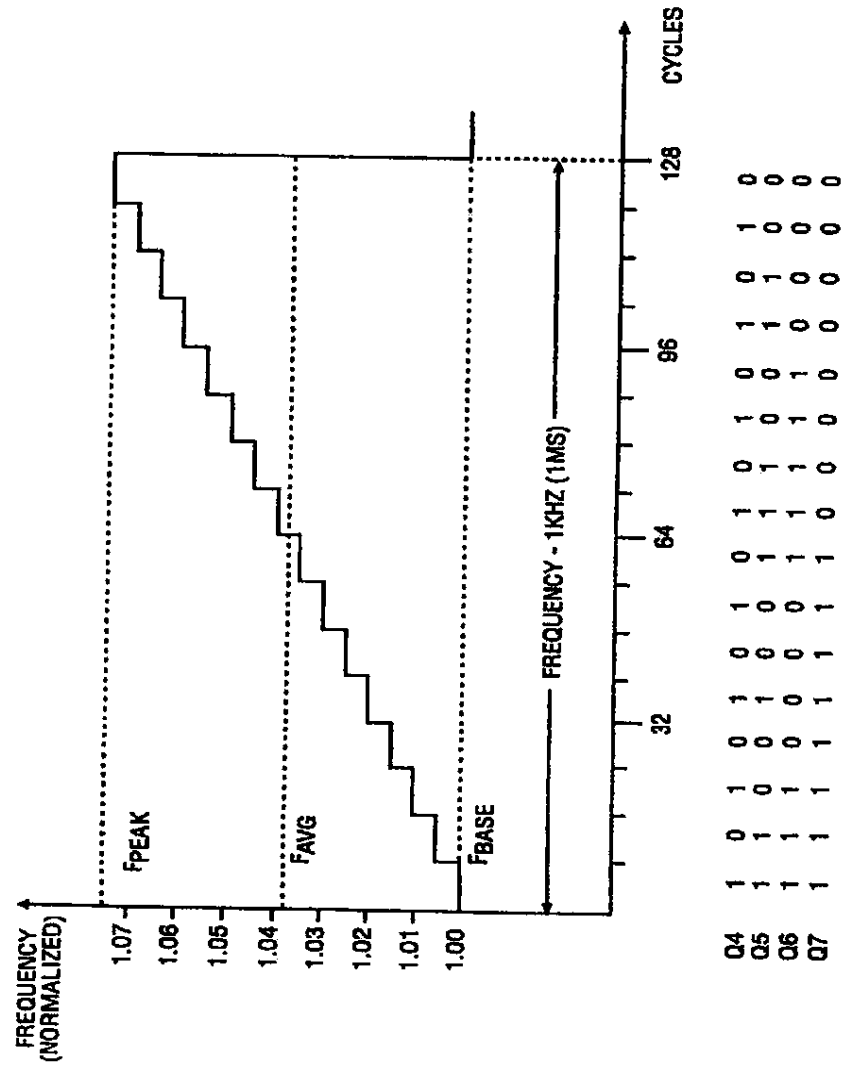


FIG. 2

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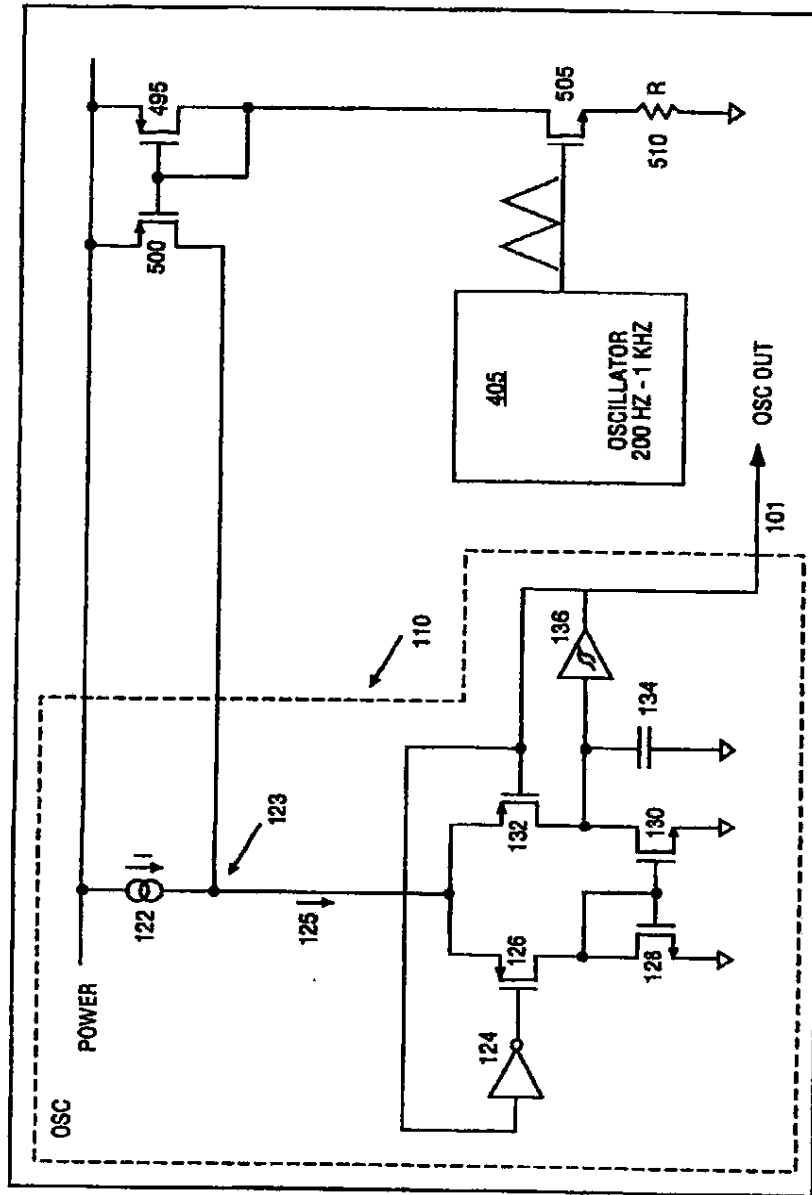


FIG. 3

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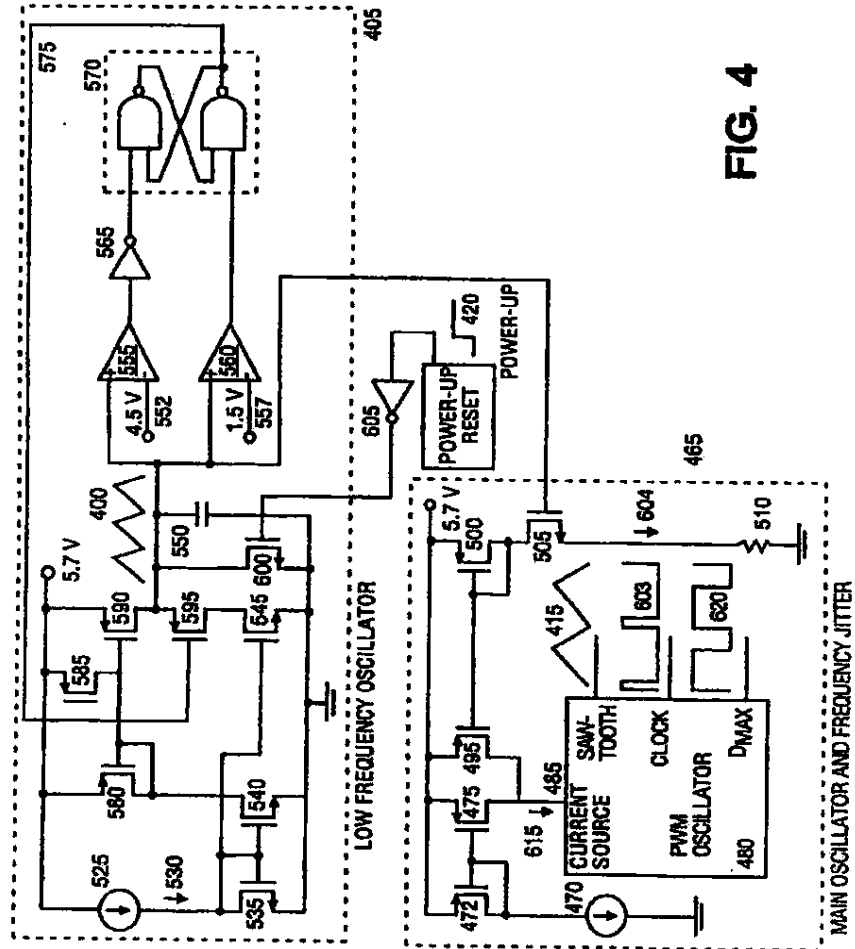


FIG. 4

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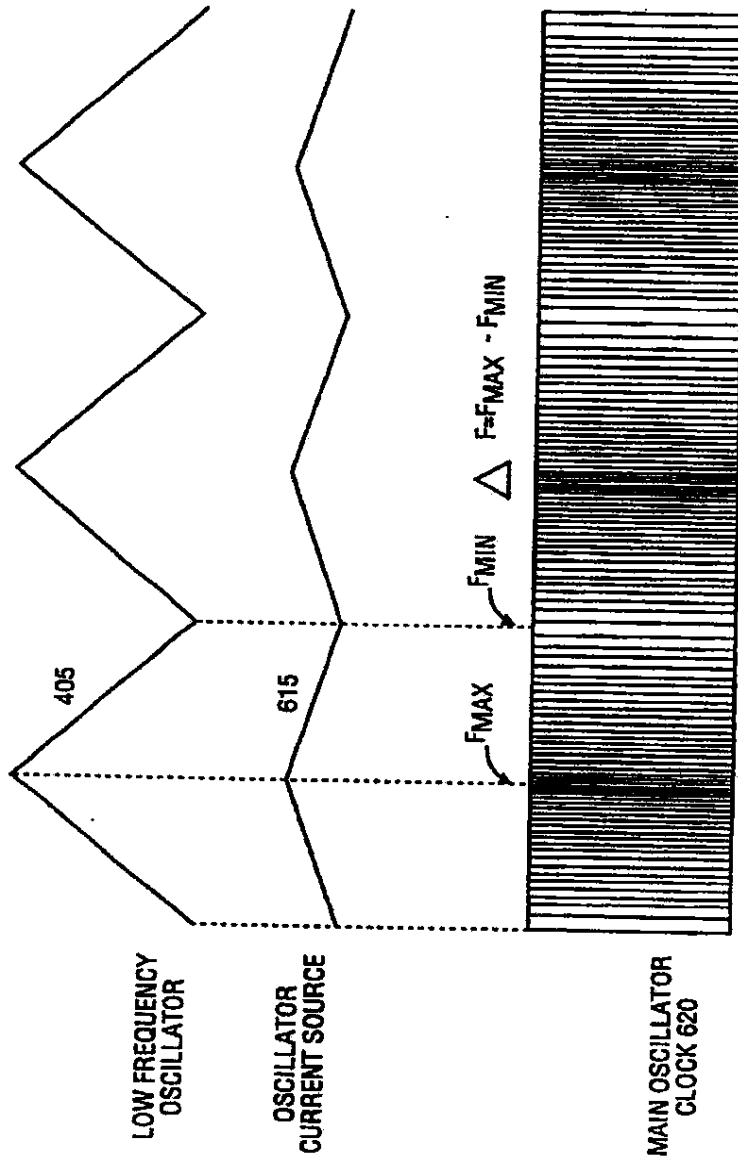
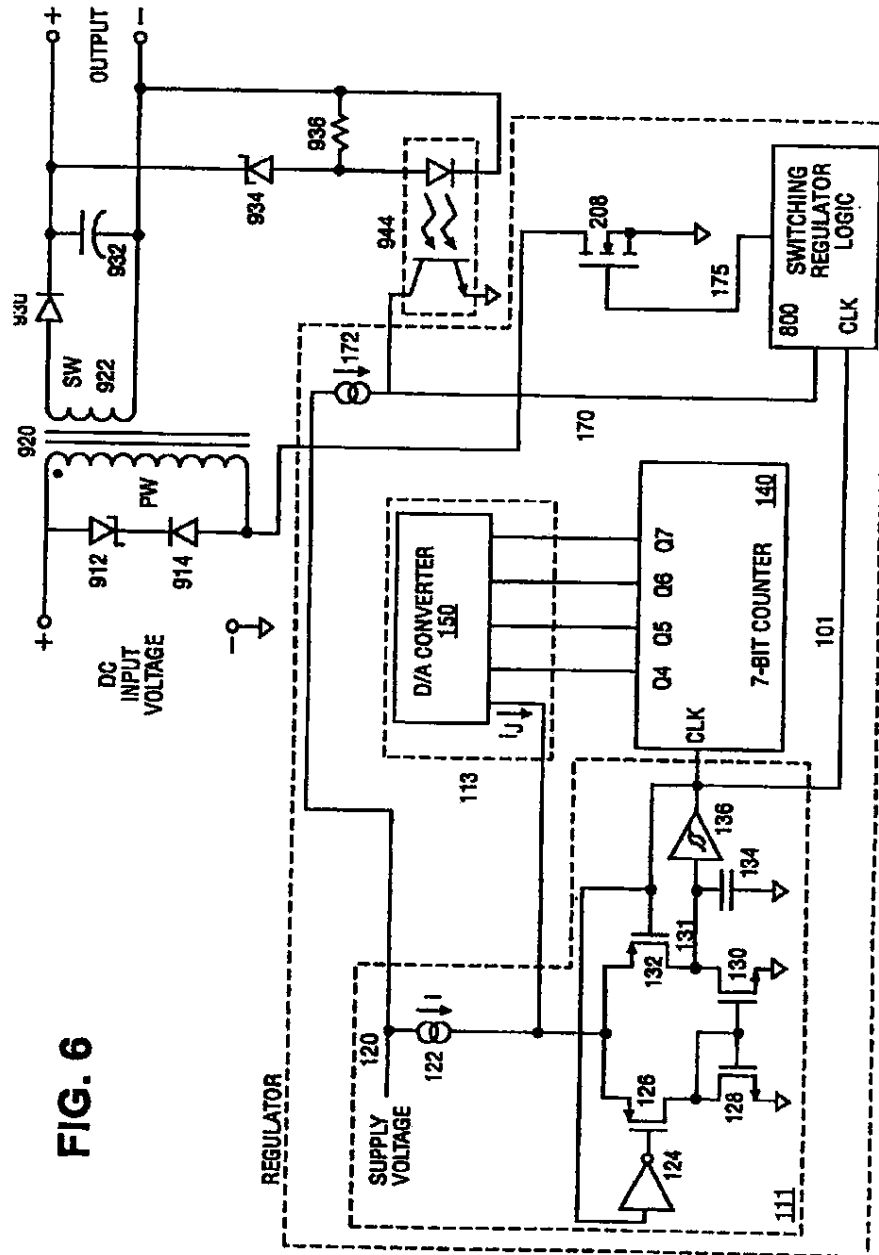


FIG. 5

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**FIG. 6**



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# FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

## BACKGROUND

The present invention relates to an off-line switched mode control system with frequency jittering.

Many products rely on advanced electronic components to cost-effectively provide the product with the desired functionality. These electronic components require power regulation circuitry to supply them with a clean and steady source of power. The development of switched mode power supply technology has led to power supplies operating at high frequency to achieve small size and high efficiency. Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternatively a variable frequency (such as in a ringing choke power supply).

Due to the high frequency operation relative to the frequency of an alternating current (AC) power line, switched mode power supplies can exacerbate problems associated with electromagnetic interference (EMI). EMI noise is generated when voltage and current are modulated by the switching power supply. This electrical noise can be transferred to the AC power line.

In addition to affecting the operation of other electronics within the vicinity of the power supply by conduction, EMI induced noise on a power line may radiate or leak from the power line and affect equipment which is not even connected to the power line. Both conducted and radiated electrical noise may adversely affect or interfere with the operation of the electronic equipment. For example, EMI noise generated by the switching power supply can cause problems for communication devices in the vicinity of the power supply. Radiated high frequency noise components may become a part of the AC mains signal and may be provided to other devices in the power grid. Further, power supply radiated EMI can interfere with radio and television transmissions.

To address EMI related interference, several specifications have been developed by government agencies in the United States and in the European Community. These agencies have established specifications that define the maximum amount of EMI that can be produced by various classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing such supplies that conform to the specifications is to minimize EMI emission to the acceptable limits of the various specifications.

EMI may be reduced in a power supply by adding snubbers and input filters. These components reduce the noise transferred to the power line and by so doing, also reduce the electric and magnetic fields of noise generated by the power line. While these methods can reduce EMI, they usually complicate the design process as well as increase the production cost. In practice, noise filtering components are added in an ad hoc manner and on a trial-and-error basis during the final design process when EMI is found to exceed the compliance limits specified by the regulatory agencies. This inevitably adds unexpected costs to the products.

Further, extra components can undesirably increase the size and weight of the power supply and thus the resulting product.

## SUMMARY OF THE INVENTION

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. In one aspect, a

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frequency jittering circuit varies the switching frequency using an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency. A digital to analog converter is connected to the control input for varying the switching frequency, and a counter is connected to the output of the oscillator and to the digital to analog converter. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency.

Implementations of the invention include one or more of the following. The oscillator has a primary current source connected to the oscillator control input. A differential switch may be used with first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and one or more comparators may be connected to the junction. The digital to analog converter has one or more current sources, with a transistor connected to each current source and to the counter. The primary current source may generate a current  $I$  and each of the current sources may generate a current lower than  $I$ . The current sources may generate binary weighted currents. The largest current source may generate a current which is less than about 0.1 of  $I$ .

In a second aspect, a method for generating a switching frequency in a power conversion system includes generating a primary current; cycling one or more secondary current sources to generate a secondary current which varies over time; and supplying the primary and secondary currents to a control input of an oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. A counter may be clocked with the output of the oscillator. The primary current may be generated by a current source. If the primary current is  $I$ , each of the secondary current sources may generate a supplemental current lower than  $I$  and which is passed to the oscillator control input. The supplemental current may be binary-weighted. The largest supplemental current may be less than approximately 0.1 of  $I$ .

In another aspect, a method for generating a switching frequency in a power conversion system includes generating a primary voltage; cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and supplying the primary and secondary voltages to a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. Where the primary voltage is  $V$ , each of the secondary voltage sources may generate a supplemental voltage lower than  $V$  which may be passed to the voltage-controlled oscillator. The supplemental voltage may be binary-weighted.

In another aspect, a frequency jittering circuit for varying a power supply switching frequency includes an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency; and means connected to the control input for varying the switching frequency.

Implementations of the invention include one or more of the following. The means for varying the frequency may include one or more current sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more current sources. The oscillator may include a primary current source connected to the control

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input; and a differential switch connected to the primary current source. The differential switch may have first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and a comparator may be connected to the junction. If the primary current source generates a current  $I$ , each of the current sources may generate a second current lower than the current  $I$ , further comprising a transistor connected to each current source connected to the counter. The means for varying the frequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source. The means for varying the frequency may include a capacitor; a current source adapted to charge the capacitor; and means for alternately charging and discharging the capacitor. One or more comparators may be connected to the capacitor and the means for alternately charging and discharging the capacitor.

In yet another aspect, a power supply includes a transformer, an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. The power supply also includes a digital to analog converter connected to the control input, the analog to digital converter having one or more current sources, wherein the primary current source generates a current  $I$  and each of the current sources generates a current lower than  $I$ . A counter is connected to the output of the oscillator and to the current sources of the digital to analog converter. Further, a power transistor is connected to the primary winding of the transformer so that when the power transistor is modulated, a regulated power supply output is provided.

In another aspect, a power supply includes a transformer connected to an input voltage. The power supply includes an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including: a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. A circuit for varying the frequency is connected to the control input, the circuit having a capacitor; a current source adapted to charge and discharge the capacitor; one or more comparators connected to the capacitor to the current source for alternately charging and discharging the capacitor. Further, a power transistor is connected to the oscillator and to the primary winding. The power transistor modulates its output in providing a regulated power supply output.

Advantages of the invention include one or more of the following. The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment. By changing the oscillator frequency back and forth, the average noise measured by the EMI measurement equipment is reduced considerably.

Further, the invention provides the required jittering without requiring a large area on the regulator chip to implement

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a capacitor in a low frequency oscillator. Further, the invention minimizes effects caused by leakage current from transistors and capacitors associated with a low frequency oscillator. Thus, the jittering operation can be maintained even at high temperature which can increase current leakage.

Additionally, the invention reduces the need to add extra noise filtering components associated with the EMI filter. Therefore a compact and inexpensive power supply system can be built with minimal EMI emissions.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a digital frequency jittering device.

FIG. 2 is a plot illustrating the operation of the device of FIG. 1.

FIG. 3 is a schematic diagram of an analog frequency jittering device.

FIG. 4 is a schematic diagram of an implementation of the device of FIG. 3.

FIG. 5 is a timing diagram illustrating the operation of the frequency jitter device of FIG. 4.

FIG. 6 is a schematic diagram of a switched mode power supply in accordance with the present invention.

#### DESCRIPTION

FIG. 1 shows a digital frequency jittering circuit 100. The digital frequency jittering circuit 100 has a primary oscillator 110 which provides a clock signal to a counter 140. The primary oscillator 110 typically operates between 100 kHz and 130 kHz. The counter 140 can be a seven bit counter. Each output of counter 140, when clocked by primary oscillator 110, represents a particular time interval. The outputs of the counter 140 are provided to a series of frequency jittering current sources 150. The outputs of the series of frequency jittering current sources 150 are presented to the primary oscillator 110 to vary its frequency, as will be described below.

Primary oscillator 110 contains a primary current source 122 which provides a primary current (denoted as  $I$ ) to node 123. Current 125 to the node 123 is provided to the source of MOSFET transistors 126 and 132. The drain of MOSFET transistor 126 is connected to the drain of an n-channel MOSFET transistor 128. The source of transistor 128 is grounded, while the gate of the transistor 128 is connected to its drain. The gate of the transistor 128 is also connected to the gate of an n-channel MOSFET transistor 130. The source of the transistor 130 is grounded while the drain is connected to the drain of the MOSFET transistor 132 at a node 131. Transistors 126, 128, 130 and 132 form a differential switch. The output of comparator 136 is connected to the gate of the transistor 132 and to an inverter 124. The output of inverter 124 is connected to the gate of transistor 126. The comparator 136 has an input which is connected to node 131 and to a capacitor 134. In combination, the transistors 126, 128, 130 and 132, capacitor 134, inverter 124, current source 122 and comparator 136 form an oscillator. The output of the comparator 136 is provided as an oscillator output OSC\_OUT 101 and is also used to drive the clock input of counter 140.

Counter 140 has a plurality of outputs Q1-Q3 (not shown) which are not used. The remaining outputs Q4-Q7 are connected to a digital-to-analog (D-to-A) converter 150, which may be implemented as a series of frequency jittering voltage sources or current sources. A Q4 output 155 is connected to the gate of a p-channel MOSFET transistor

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154. A Q5 output 157 is connected to the gate of a p-channel MOSFET transistor 158. The Q6 output 163 is connected to the gate of a p-channel MOSFET transistor 162, and Q7 output 167 is connected to the gate of a p-channel MOSFET transistor 166. When D-to-A converter 150 is viewed as a plurality of current sources, the source of transistor 154 is connected to a jittering current source 152, which provides a current which is  $\frac{1}{200}$ th of the current I generated by the current source 122. The source of MOSFET transistor 158 is connected to a current source 156 which provides a current that is  $\frac{1}{200}$ th of the current I. The source of the MOSFET transistor 162 is connected to a jittering current source 160 which provides a current that is  $\frac{1}{200}$ th of I. Finally, the source of the MOSFET transistor 166 is connected to a jittering current source 164 which provides a current that is  $\frac{1}{200}$ th of the current I. The current sources 152, 156, 160 and 164 are binary-weighted, that is, the current source 164 provides twice the current provided by the current source 160, the current source 160 provides twice the current supplied by the current source 156 and the current source 156 provides twice the current provided by the current source 152.

Further, in one embodiment, the largest current source 164 may supply no more than 10% of the current I provided by the primary current source 122. The drain of transistors 154, 158, 162 and 166 are joined together such that the supplemental frequency jittering current sources of the D-to-A converter 150 can be provided to supplement the primary current source 122.

During operation, at every eight clock cycles, the counter output Q4 on line 153 changes state. Similarly, at every 16 clock cycles, the output Q5 on line 157 changes state and at every 32 clock cycles, the output Q6 on line 163 changes state, and every 64 clock cycles, the output Q7 on line 167 changes state. The entire counting cycle thereafter repeats itself.

Each time the output Q4 on line 153 is low, transistor 154 is turned on to inject current in the amount of  $I/200$  to node 123 so that the total current 125 is 1.005I. Similarly, each time that the output Q5 on line 157 is low, transistor 158 is turned on to inject current in the amount of  $I/200$  to node 123 so that the total current 125 is 1.01I. Further, each time that output Q6 on line 163 is low, transistor 162 is turned on to inject current in the amount of  $I/200$  to node 123 so that the total current 125 is 1.02I. Finally, each time that the output Q7 on line 167 is low, the transistor 166 is turned on to inject current in the amount of  $I/200$  to node 123 so that the total current 125 is 1.04I.

Additionally, when combinations of outputs Q4-Q7 are turned on, the outputs of the respective current sources 152, 156, 160 and 164 are added to the output of current source 122 to vary the frequency of the primary oscillator 110. In this manner, counter 140 drives a plurality of current sources to inject additional current to the main current source 122 such that the frequency of the primary oscillator 110 is varied.

The jittering operation of the embodiment of FIG. 1 is further illustrated in a chart in FIG. 2. A normalized operating frequency is plotted on the y-axis while the counting cycle as shown by the counter outputs Q4-Q7 is plotted on the x-axis. As shown in FIG. 2, as the counter counts upward to the maximum count of 128, the peak switching frequency is achieved. This peak switching frequency is normalized to be about 1.075 times the base switching frequency. Further, on average, the switching frequency is between 1.03 and 1.04 times the base switching frequency. Thus, the embodiment of FIG. 1 deviates the switching frequency of the

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oscillator within a narrow range. This deviation reduces EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment such that the noise measured by the EMI test equipment is reduced considerably.

FIG. 3 shows an analog frequency jittering circuit. More details on the analog frequency jittering device are shown in co-pending U.S. application Ser. No. 09/080,774, entitled "OFFLINE CONVERTER WITH INTEGRATED SOFT START AND FREQUENCY JITTER," filed on May 18, 1998, the content of which is hereby incorporated by reference. In FIG. 3, the primary oscillator 110 provides an oscillator output on line OSC-OUT 101. An analog low frequency oscillator 405 is also provided. Primary oscillator 110 typically operates between a range of 30 to 300 kHz, while the low frequency oscillator 405 typically operates between a range of 5 Hz to 5 kHz. As discussed above, the switching frequency of the primary oscillator 110 is determined by the amount of current the primary oscillator uses to charge and discharge capacitor 134. The low frequency oscillator 405 varies this current within a narrow range to jitter the frequency of the primary oscillator 110.

The output of low frequency oscillator 405 is provided to a MOSFET transistor 505 connected to a resistor 510 and a current mirror including transistors 495 and 500. Transistor 500 is connected to node 123 so that extra current can be added to current source 122 feeding the primary oscillator. In this manner, the frequency of the primary oscillator 110 is shifted around a narrow range to reduce the EMI noise.

FIG. 4 shows a more detailed implementation of FIG. 3. As shown therein, main oscillator 465 has a current source 470 that is mirrored by current mirror transistors 472 and 475. Main oscillator drive current 615 is provided to current source input 485 of oscillator 480. The magnitude of the current input into current source input 485 determines the frequency of the oscillation signal 415 provided by oscillator 480. In order to vary the frequency of the oscillation signal 415, an additional current source 495 is provided within the main oscillator 465. The current source 495 is mirrored by current source mirror 500.

The current provided by current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases, so does the voltage at the source of main oscillator transistor 505 due to the increasing voltage at the gate of the transistor 505 and the relatively constant voltage drop between the gate and source of the transistor 505. As the voltage at the source of transistor 505 increases, so does the current 604 flowing through the resistor 510. The current flowing through the resistor 510 is the same as the current flowing through additional current source 500 which mirrors transistor 495.

Since the frequency variation signal 400 is a triangular waveform having a fixed period, as shown, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency will linearly rise to a peak and then fall to its lowest value. In this way, the current 615 provided to current source input 485 of the oscillator 480 is varied in a known fixed range that allows for an easy and accurate frequency spread of the high frequency current. Further, the variance of the frequency is determined by the magnitude of the current provided by current source mirror 500, which is a function of the resistance of the resistor 510.

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Frequency variation circuit 405 includes a current source 525 that produces a fixed magnitude current 530 that determines the magnitude of the frequency of the frequency variation signal 400. Although the current 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current. If such variable current is generated, the frequency spread is not fixed in time but varies with the magnitude of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirrored by second transistor 540 and third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of the capacitor 550. Frequency variation circuit capacitor 550 has a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of low frequency oscillator 405. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 560. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage on line 552 which is about 4.5 volts. The output of lower limit comparator 560 will be low when the magnitude of frequency variation signal 400 drops below lower threshold voltage on line 557 which is about 1.5 volts. The output of upper limit comparator 555 is provided to the frequency variation circuit inverter 565 the output of which is provided to the reset input of frequency variation circuit latch 570. The set input of frequency variation circuit latch 570 receives the output of lower limit comparator 560.

In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between the upper threshold on line 552, 4.5 volts, and lower threshold on line 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation signal 400 exceeds upper level threshold on line 552. This means that the reset input will receive a high signal when the magnitude of the frequency variation signal 400 rises above the upper threshold signal on line 552.

The charge signal 575 output by frequency variation circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal on line 552. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 585 and 595, current can flow into the capacitor 550, which steadily charges capacitor 550 and increases the magnitude of frequency variation signal 400. The current that flows into the capacitor 550 is derived from current source 525 because the current through transistor 590 is mirrored from transistor 580, which in turn is mirrored from transistor 535.

During power up, when power-up signal 420 is low, the output of inverter 605 is high, which turns on transistor 600, causing frequency variation signal 400 to go low. The frequency variation signal 400 starts from its lowest level to perform a soft start function during its first cycle of operation.

Referring to FIGS. 4 and 5, FIG. 5 shows the operation of the analog frequency jittering device of FIG. 4. In FIG. 5, a frequency variation signal 485 is provided to the main oscillator 465. The magnitude of the current 615 is approximately the magnitude of the frequency variation signal 405, less the threshold voltage of transistor 585, and divided by the resistance of the resistor 510 plus the magnitude of the current produced by the current source 475. The current 615 varies with the magnitude of the frequency variation signal 485. The variation of the current 615 in turn varies the frequency of the oscillator clock.

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Referring now to FIG. 6, a switched mode power supply is shown. Direct current (DC) input voltage is provided to a Zener diode 912 which is connected to a diode 914. The diodes 912-914 together are connected in series across a primary winding of a transformer 920. A secondary winding 922 is magnetically coupled to the primary winding of transformer 920. One terminal of the secondary winding 922 is connected to a diode 930, whose output is provided to a capacitor 932. The junction between diode 930 and capacitor 932 is the positive terminal of the regulated output. The other terminal of capacitor 932 is connected to a second terminal of the secondary winding and is the negative terminal of the regulated output. A Zener diode 934 is connected to the positive terminal of the regulated output. The other end of Zener diode 934 is connected to a first end of a light emitting diode in an opto-isolator 944. A second end of the light-emitting diode is connected to the negative terminal of the regulated output. A resistor 936 is connected between the negative terminal of the regulated output and the first end of the light-emitting diode of opto-isolator 944. The collector of the opto-isolator 944 is connected to current source 172. The output of current source 172 is provided to the switching regulator logic 800.

Connected to the second primary winding terminal is the power transistor 208. Power transistor 208 is driven by the switching regulator logic 800. Switching regulator logic 800 receives a clock signal 101 from an oscillator 111. A counter 140 also receives the clock signal 101 from the primary oscillator 111. The outputs of counter 140 are provided to D-to-A converter 150, which is connected to oscillator 111 for jittering the oscillation frequency. Alternatively, in lieu of counter 140 and a D-to-A converter 150, an analog low frequency jittering oscillator may be used.

The foregoing disclosure and description of the invention are illustrative and explanatory thereof, and various changes in the size, shape, materials, components, circuit elements, wiring connections and contacts, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit of the invention.

What is claimed is:

1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:
  - an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;
  - a digital to analog converter coupled to the control input for varying the switching frequency; and
  - a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.
2. The circuit of claim 1, wherein the oscillator further comprises a primary current source coupled to the oscillator control input.
3. The circuit of claim 2, further comprising a differential switch, including:
  - first and second transistors coupled to the primary current source;
  - a third transistor coupled to the first transistor; and
  - a fourth transistor coupled to the second transistor at a junction.
4. The circuit of claim 3, further comprising a capacitor coupled to the junction.
5. The circuit of claim 3, further comprising one or more comparators coupled to the junction.

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6. The circuit of claim 2, wherein the digital to analog converter has one or more secondary current sources.

7. The circuit of claim 6, further comprising a transistor coupled between each secondary current source and the counter.

8. The circuit of claim 6, wherein the primary current source generates a current  $I$  and each of the secondary current sources generates a current lower than  $I$ .

9. The circuit of claim 8, wherein the secondary current sources generate binary weighted currents.

10. The circuit of claim 8, wherein the largest secondary current source generates a current which is less than about 0.1 of  $I$ .

11. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary current;

cycling one or more secondary current sources to generate a secondary current which varies over time; and

combining the secondary current with the primary current to be received at a control input of an oscillator for generating a switching frequency which is varied over time.

12. The method of claim 11 further comprising the step of clocking a counter with the output of the oscillator.

13. The method of claim 11 wherein the primary current is generated by a current source.

14. The method of claim 11 wherein the primary current is  $I$  and each of the secondary current sources generates a supplemental current lower than  $I$ , and further comprising passing the supplemental current to the oscillator control input.

15. The method of claim 14 further comprising binary-weighting the supplemental current.

16. The method of claim 14 wherein the largest supplemental current is less than approximately 0.1 of  $I$ .

17. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary voltage;

cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and

combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

18. The method of claim 17 further comprising clocking a counter with the output of the oscillator.

19. The method of claim 17 wherein the primary voltage is  $V$  and each of the secondary voltage sources generates a supplemental voltage lower than  $V$ , further comprising passing the supplemental voltage to the voltage-controlled oscillator.

20. The method of claim 19, wherein the supplemental voltage is binary-weighted.

21. A frequency jittering circuit for varying a power supply switching frequency, comprising:

an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency; and

means coupled to the control input for varying the switching frequency, including:

one or more current sources coupled to the control input; and

a counter coupled to the output of the oscillator and to the one or more current sources.

22. The circuit of claim 21 wherein the oscillator further comprises:

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a primary current source coupled to the control input; and a differential switch coupled to the primary source.

23. The circuit of claim 22 wherein the oscillator further comprises:

first and second transistors coupled to the primary current source;

a third transistor coupled to the first transistor; and

a fourth transistor coupled to the second transistor at a junction.

24. The circuit of claim 22 further comprising a capacitor and a comparator coupled to the junction.

25. The circuit of claim 22 wherein the primary current source generates a current  $I$  and each of said one or more current sources generates a current lower than  $I$ .

26. The circuit of claim 22 wherein the primary current source generates a current  $I$  and each of said one or more current sources generates a second current lower than the current  $I$ , further comprising a transistor coupled to each current source connected to the counter.

27. The circuit of claim 21 further comprising a transistor coupled to each current source and to the counter.

28. The circuit of claim 21 wherein the oscillator further comprises:

a primary voltage source coupled to the control input; and a differential switch coupled to the primary voltage source.

29. The circuit of claim 21 wherein the means for varying the frequency further comprises:

a capacitor; and

a current source adapted to charge and discharge the capacitor.

30. The circuit of claim 29 further comprising:

one or more comparators coupled to the capacitor; and means coupled to the capacitor for alternately charging and discharging the capacitor.

31. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input; a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and a comparator coupled to the differential switch;

a digital to analog converter coupled to the control input, the digital to analog converter having one or more current sources, wherein the primary current source generates a current  $I$  and each of said one or more current sources generates a current lower than  $I$ ;

a counter coupled to the output of the oscillator and to the current sources of the digital to analog converter; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

32. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input; a differential switch coupled to the primary current source;

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a capacitor coupled to the differential switch; and  
a comparator coupled to the differential switch  
a circuit for varying the frequency, the circuit coupled to  
the control input, including:  
a capacitor;  
a current source adapted to charge and discharge the  
capacitor;  
one or more comparators coupled to the capacitor and  
coupled to the current source for alternatingly charging  
and discharging the capacitor; and

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a power transistor coupled to the oscillator and to one  
terminal of the primary winding, the power transistor  
modulating its output in providing a regulated power  
supply output.

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FCS0000013

# EXHIBIT G



# 5.00 - 216 - 253

 Case Docket No. SS-520-01  
 Date April 7, 1988
In re application of: Klas H. EklundSerial No.: 07/041,994Filed: April 24, 1987For: HIGH VOLTAGE MOS TRANSISTORSCOMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

- ☐ No additional fee is required. ☒ Two Month Extension Fee Enclosed. (\$85.00)
- ☐ Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addnl. Fee
Total Claims	_____	Minus	_____	_____ x	\$12.00	_____
Indep. Claims	_____	Minus	_____	_____ x	\$34.00	_____

Additional Fee Due \$ \_\_\_\_\_

- ☒ A verified statement claiming small entity status ☒ has been filed; \_\_\_\_\_ is attached. The fee due is fifty percentum of the above.

Fee Due \$ \_\_\_\_\_

- ☒ A check in the amount of \$ 85.00 is attached. (Two Month Extension Fee)

- ☒ Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

 040 04/13/88 041994  
 Attorney For Applicant

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 By: [Signature]  
 Reg. No.: 22,617

 I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88.

 (Date of Deposit)  
Thomas E. Schatzel  
[Signature] 4/7/88

FCS0000166



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Serial No.: 07/041,994

Filed : 04-24-87

For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit 253

Examiner: J. Jackson

Attorneys Docket No.:  
SS-520-01

COMMISSIONER OF PATENTS  
& TRADEMARKS  
Washington, D.C. 20231

Date of this Paper:

April 7, 1988

#### AMENDMENT

In response to the U.S. Patent Office Action mailed December 7, 1987 (Paper No. 2), please amend this application as follows:

#### In the Specification

Page 1, line 26, change "of" to --on--;

Page 9, line 15, insert the following paragraph:

--It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one complimentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.--

I hereby certify that this correspondence is being deposited with the United States Postal Service at first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88 (Date of Deposit)

Thomas E. Schatzel

Signature Date 4/7/88

FCS0000167

Page 9, line 28, change "72" to --73--.

In the Claims

Cancel claims 1-5 and 8-18.

Add new claims 19-23 as follows:

19. A high voltage MOS transistor comprising:
- a semiconductor substrate of a first conductivity type having a surface,
  - a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,
  - a source contact connected to one pocket,
  - a drain contact connected to the other pocket,
  - an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,
  - a <sup>surface adjoining</sup> layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,
  - said top layer of material and said substrate being subject to application of a reverse-bias voltage,
  - an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region,
  - and
  - a gate electrode on the insulating layer and electrically isolated from the <sup>substrate</sup> region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

19.23

20.<sup>4</sup> The high voltage MOS transistor of claim 19 having one channel conductivity type in combination with a ~~complementary~~ <sup>complementary</sup> high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

21.<sup>5</sup> The high voltage MOS transistor of claim 19 combined on the same chip with a low voltage CMOS implemented device.

22.<sup>4</sup> The combination of claim 21 further including,  
 a ~~complementary~~ <sup>complementary</sup> high voltage MOS transistor, and  
 a ~~complementary~~ <sup>complementary</sup> low voltage CMOS implemented device on the same chip and isolated from each other.

23.<sup>7</sup> A high voltage MOS transistor comprising:  
 a semiconductor substrate of a first conductivity type having a surface,  
 a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,  
 a source contact connected to one pocket,  
 an extended source region of the second conductivity type extending laterally each way from the source contact pocket to ~~surface-adjointing position,~~ <sup>positions</sup> surface-adjointing positions,  
 a layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjointing positions,  
 said top layer and said substrate being subject to application of a reverse-bias voltage,  
 a drain contact connected to the other pocket,

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b<sub>1</sub> an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-<sup>surface adjoining</sup> adjoining positions,  
 b<sub>2</sub> a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-<sup>surface adjoining</sup> adjoining positions,

b<sub>3</sub> said top layer of material and said substrate being subject to application of a reverse-bias voltage,

b<sub>4</sub> an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-<sup>surface adjoining</sup> adjoining positions of the extended source region and the extended drain region, and

b<sub>5</sub> a gate electrode on the insulating layer and electrically isolated from the <sup>substrate</sup> region thereunder which forms a channel laterally between the nearest surface-<sup>surface adjoining</sup> adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

Amend the claims as follows:

Claim 6, line 1, change "5" to --19--; and

Claim 7, line 1, change "5" to --19--.

#### REMARKS

The specification has been amended to correct minor errors and to provide an antecedent basis in the specification for epitaxial layer and epi-island mentioned in former claims 11 and 13.

This invention relates to high voltage, metal oxide semiconductor transistors of the field effect type. There is a need for more efficient transistors which can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The

integrated devices should be easily combined with low voltage (five volt) control logic on the same chip. Devices of opposite conductivity should be combinable in a complimentary manner on the same chip. Such transistors, with modifications, should be capable of source-follower applications.

The applicant has disclosed a novel and unobvious high voltage MOS transistor having a low threshold voltage that is compatible with five volt control logic and a low ON-resistance. This transistor can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The high voltage MOS transistors can be modified for source-follower applications by providing both extended source regions and extended drain regions. These transistors are formed on a substrate of a first conductivity type having a surface. A pair of laterally spaced pockets of semiconductor material of a second conductivity type are provided within the substrate and adjoining the substrate surface. A source contact is connected to one pocket and a drain contact is connected to the other pocket. An extended drain region of a second conductivity type extends laterally each way from the drain pocket to surface-adjoining positions. A layer of material of the first conductivity type is provided on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The top layer of material and the substrate are subject to application of a reverse-bias voltage. None of the cited references show such structure.

Colak, U.S. Patent No. 4,626,879, shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain



region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom epitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediate epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON" resistance.

Thomas, U.S. Patent No. 4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

The claims are now clearly distinguished from the cited references. New claim 19 recites "an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjointing positions, a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjointing positions". When high voltage n-channel and p-channel devices are combined on the same chip with low voltage control logic, this structure isolates the devices from each other. Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage. The structure of claim 19 enables a lower threshold voltage, compatibility with five volt control logic, and eliminates the need for an additional power supply and interface circuit.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and thus, can be distinguished for the same reasons as claim 19.

Claim 23 is directed to the transistor, shown in Fig. 5 of the drawings, that has been modified for source-follower applications by providing both extended source and drain regions. Top layers cover intermediate portions of the extended source and drain regions. The top layers and substrate are subject to application of a reverse-bias voltage.

Accordingly, claims 6-7 and 20-23 are patentably distinct from the cited references and allowance of these claims is requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney would expedite matters, such a conference is invited.

Respectfully submitted,

Reg. No. 22,611

By Thomas E. Schatzel  
Thomas E. Schatzel

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Wash.

ington, D.C. 20231, on 4-7-88  
(Date of Deposit)  
Thomas E. Schatzel  
Thomas E. Schatzel  
Signature Date

FCS0000173

Serial No.: 07/041,994  
Filed: 4-24-87  
Attlys. Docket No.: SS-520-01

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

\_\_\_ other than a small entity

\_\_\_ verified statement attached

X small entity

X verified statement already filed

Payment of fees

X The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please \_\_\_ also charge issues fees under 37 C.F.R. 1.18  
X do not  
to Account No. 19-0310.

Reg. No. 22,611

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Attorney for Applicant

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Thomas E. Schatzel  
*Thomas E. Schatzel*  
Signature Date 4/7/88

FCS0000174

# **EXHIBIT H**

#6  
PATENTHAND CARRIED TO PTOCase Docket No. SS-520-01Date August 12, 1988In re application of: Klas H. EklundSerial No.: 07/041,994Filed: April 24, 1987For: HIGH VOLTAGE MOS TRANSISTORSATTN: BOX A.F.  
COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment After Final for the above application.

☒ No additional fee is required.☐ Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra.	Rate	Addtl. Fee
Total Claims		Minus		x	\$12.00	=
Indep. Claims		Minus		x	\$34.00	=

Additional Fee Due \$ \_\_\_\_\_

☒ A verified statement claiming small entity status ☒ has been filed; \_\_\_\_\_ is attached. The fee due is fifty percentum of the above.

Fee Due \$ \_\_\_\_\_

☐ A check in the amount of \$ \_\_\_\_\_ is attached.☒ Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

Attorney For Applicant

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A Professional Corporation  
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(408) 727-7077

By

Reg. No.: 22,611

FCS0000184

88  
PATENT  
8/15/88

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Group Art Unit: 253

Serial No.: 07/041,994

Examiner: J. Jackson, Jr.

Filed: : April 24, 1987

Attorneys Docket No.:  
88-520-01

For : HIGH VOLTAGE MOS TRANSISTORS

ATTENTION: BOX A.F.

COMMISSIONER OF PATENTS  
& TRADEMARKS  
Washington, D.C. 20231

Date of this Paper:

August 12, 1988

AMENDMENT AFTER FINAL

In response to the U.S. Patent Office Action mailed June 17, 1988  
(Paper No. 4), please amend this application as follows:

In the Claims

- Claim 19, line 12, before "layer" insert --surface adjoining--;
- line 22, before "region" insert --substrate--.
- Claim 20, line 2, change "complimentary" to --complementary--.
- Claim 22, line 2, change "complimentary" to --complementary--;
- line 3, change "complimentary" to --complementary--.
- Claim 23, line 9, delete "a";
- line 10, change "position" to --positions--;
- line 11, before "layer" insert --surface adjoining--;
- line 18, delete "a";
- line 20, before "layer" insert --surface adjoining--;
- line 30, before "region" insert --substrate--.

REMARKS

The applicant appreciates the telephone interview on August 10, 1988, courteously granted by the Examiner.

Claim 19, as amended, now provides for an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjointing positions and a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjointing positions. The layer 16 of Colak is not surface-adjointing but is buried under layer 18. There is no layer of material of the first conductivity type on top of layer 18. Colak's layer 16 extends from beneath the drain contact pocket 24 to the channel region 20, and thus, is not between the drain contact pocket and the surface adjoining positions of the extended drain region.

Claim 19 also provides for the top layer of material and the substrate being subject to application of a reverse-bias voltage. Thus, the top layer and the substrate act as gates for controlling current flow through the extended drain region between the surface adjoining positions and the drain contact pocket. This structure can be considered a double-sided, junction-gate field-effect transistor (JFET). Colak shows a layer 14 intermediate a layer 16 and a substrate 12 that are subject to application of a reverse-bias voltage. Though this structure of Colak could be considered a double-sided JFET, layer 16 is not surface-adjointing as defined in claim 19. Colak's double-sided JFET is buried under layer 18 which is connected in parallel with layer 14 by semiconductor zones 16c, 16d. Layer 16 also acts as a gate for layer 18 so that layers 16 and 18 could be considered a single-sided JFET. Thus, the extended drain of Colak includes the single-sided JFET connected in parallel with the double-

sided JFET thereunder. Both the extended drain structure of claim 19 and Colak's drain structure have relatively high voltage capability. However, it is desirable to control the high voltage with relatively low voltage.

Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surface-adjointing position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjointing position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device. The MOSFET structure has a lower threshold voltage than a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. D-MOS devices usually require an additional power supply of ten to fifteen volts for driving the gate. The MOSFET structure has less on-resistance and thus, further reduces the total on-resistance of the combined structure (MOSFET plus double-sided JFET).

Claim 19 is directed to the structural combination of a double-sided JFET and a MOSFET so that a high voltage transistor can be controlled with relatively low voltage. Thus, claim 19 is patentably distinct over Colak.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and are thus patentably distinct from Colak for the same reasons as claim 19. While Thomas shows that high voltage FET devices are advantageously formed complementary and also integrated with low voltage devices, claims 20-22 are limited to transistors having the structure as defined in claim 19. This structure facilitates isolation of complementary high voltage devices and low voltage, C-MOS



implemented devices on the same chip. Isolation of the epitaxial layers shown by Colak from corresponding layers of a complementary device would be difficult.

Claims 6 and 7 include further limitations on the depth of the top layer and the doping density thereof. The depth is one-half or less than that disclosed by Colak for layer 16 and the doping density is at least five times greater. Furthermore, Colak's layer 16 is not similarly situated as the top layer of claim 19, and thus, is not comparable. Thus, claims 6 and 7 are patentably distinct from Colak for the same reasons as claim 19 and for the further limitations therein.

Claim 23 is directed to the transistor 63, shown in Fig. 5, that is suitable for source follower applications. This claim contains limitations similar to claim 19 for the MOSFET structure and the double-sided JFET about the drain contact pocket. It further includes structural limitations for a double-sided JFET about the source contact pocket. While the book by Sze discloses MOSFET structures having sources and drains that are similar to each other, such sources and drains are not similar to the double-sided JFET structures disclosed by the applicant and specifically claimed structurally in claim 23. Thus, claim 23 is patentably distinguished from Sze.

Should the Examiner be of the opinion that a telephone conference with applicant's attorney would be beneficial, he is invited to contact the undersigned at the number set out below.

Respectfully submitted,

Reg. No. 22,611.

By

  
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PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

☐ other than a small entity

☐ verified statement attached

☒ small entity

☒ verified statement already filed

Payment of fees

☒ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ☐ also charge issues fees under 37 C.F.R. 1.18  
☒ do not  
to Account No. 19-0310.

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FCS0000189

# **EXHIBIT I**

**REDACTED**